Lyra: A Cross-Platform Language and Compiler for Data Plane Programming on Heterogeneous ASICs

Jiaqi Gao, Ennan Zhai, Hongqiang Harry Liu, Rui Miao, Yu Zhou
Bingchuan Tian, Chen Sun, Dennis Cai, Ming Zhang, Minlan Yu

Alibaba Group 阿里巴巴集团
HARVARD UNIVERSITY
清華大學 Tsinghua University
南京大學 NANJING UNIVERSITY

Programmable switches gain significant traction

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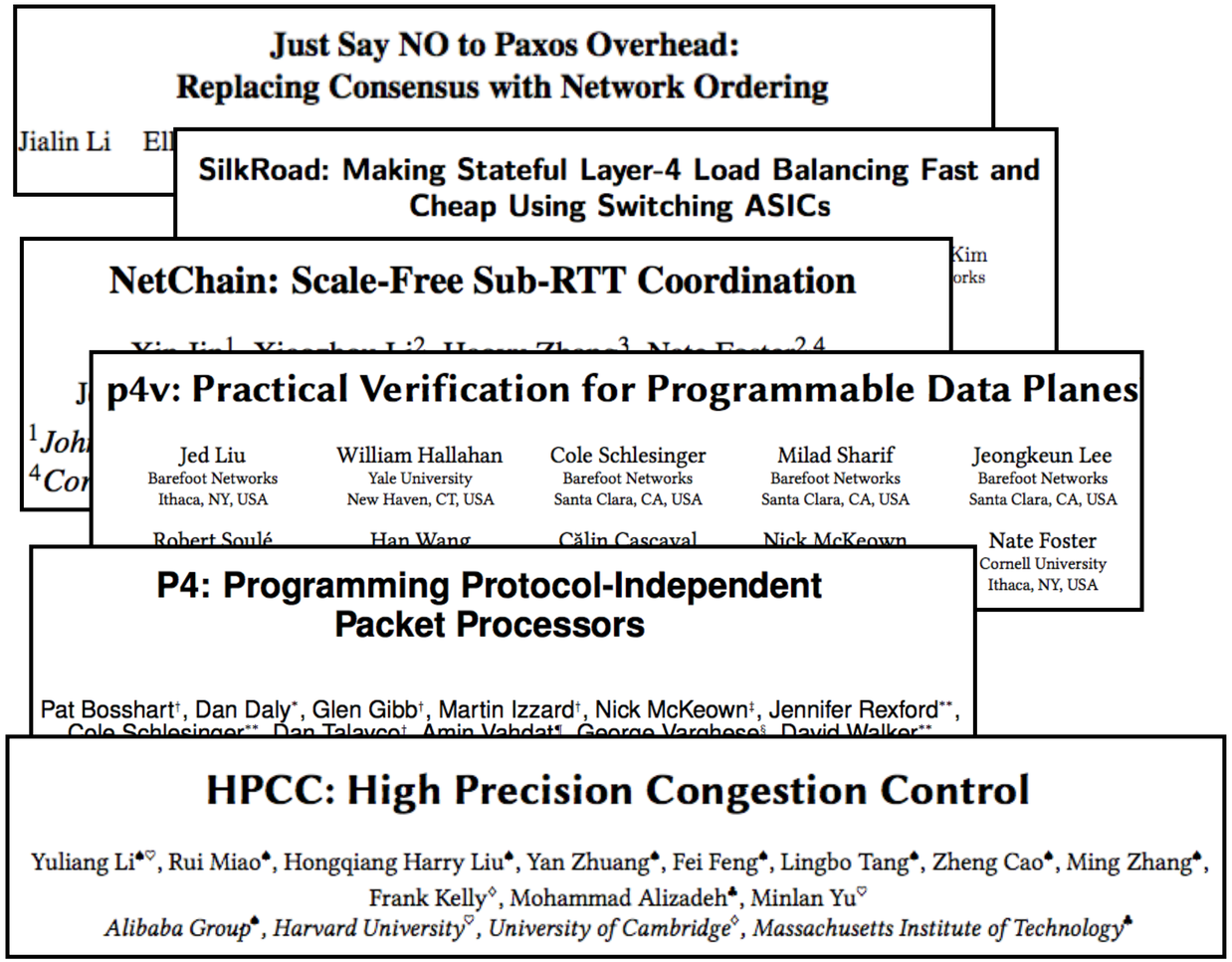

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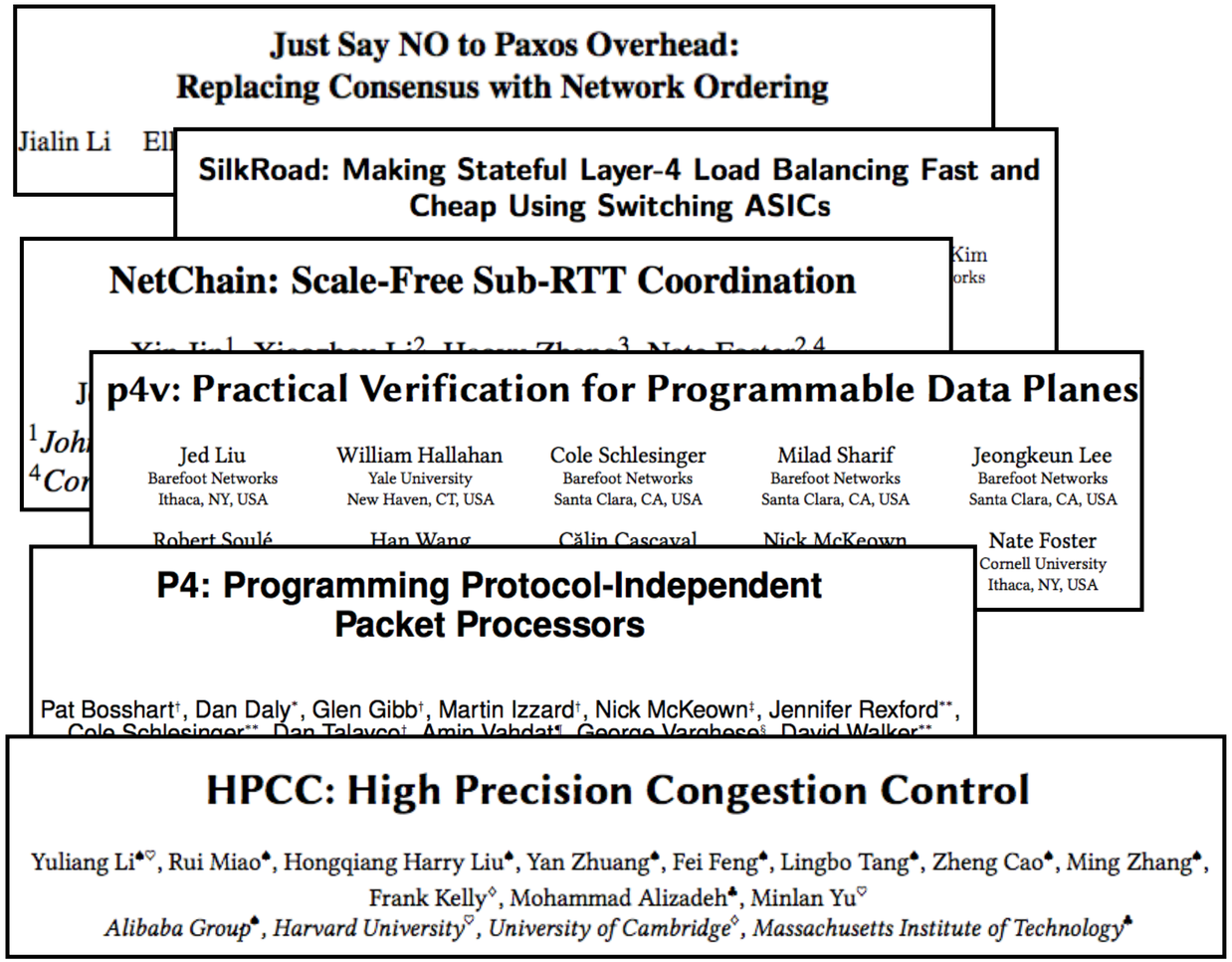

Just Say NO to Paxos Overhead:
Replacing Consensus with Network Ordering

Jialin Li El

SilkRoad: Making Stateful Layer-4 Load Balancing Fast and Cheap Using Switching ASICs

Kim
orks

NetChain: Scale-Free Sub-RTT Coordination

p4v: Practical Verification for Programmable Data Planes

Jed Liu	William Hallahan	Cole Schlesinger	Milad Sharif	Jeongkeun Lee
Barefoot Networks	Yale University	Barefoot Networks	Barefoot Networks	Barefoot Networks
Ithaca, NY, USA	New Haven, CT, USA	Santa Clara, CA, USA	Santa Clara, CA, USA	Santa Clara, CA, USA

Robert Soulé Han Wang Călin Cascaval Nick McKeown Nate Foster
Cornell University
Ithaca, NY, USA

P4: Programming Protocol-Independent Packet Processors

Pat Bosshart†, Dan Daly*, Glen Gibb†, Martin Izzard†, Nick McKeown‡, Jennifer Rexford**,

HPCC: High Precision Congestion Control

Yuliang Li♠♡, Rui Miao♠, Hongqiang Harry Liu♠, Yan Zhuang♠, Fei Feng♠, Lingbo Tang♠, Zheng Cao♠, Ming Zhang♠,
Frank Kelly♢, Mohammad Alizadeh♠, Minlan Yu♡
Alibaba Group♠, Harvard University♡, University of Cambridge♢, Massachusetts Institute of Technology♠

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Data plane programming is still at an early stage …

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Chip specific languages ~ Assembly languages

Running example: A network sequencer

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Linearizing the transactions for consensus protocols such as Paxos

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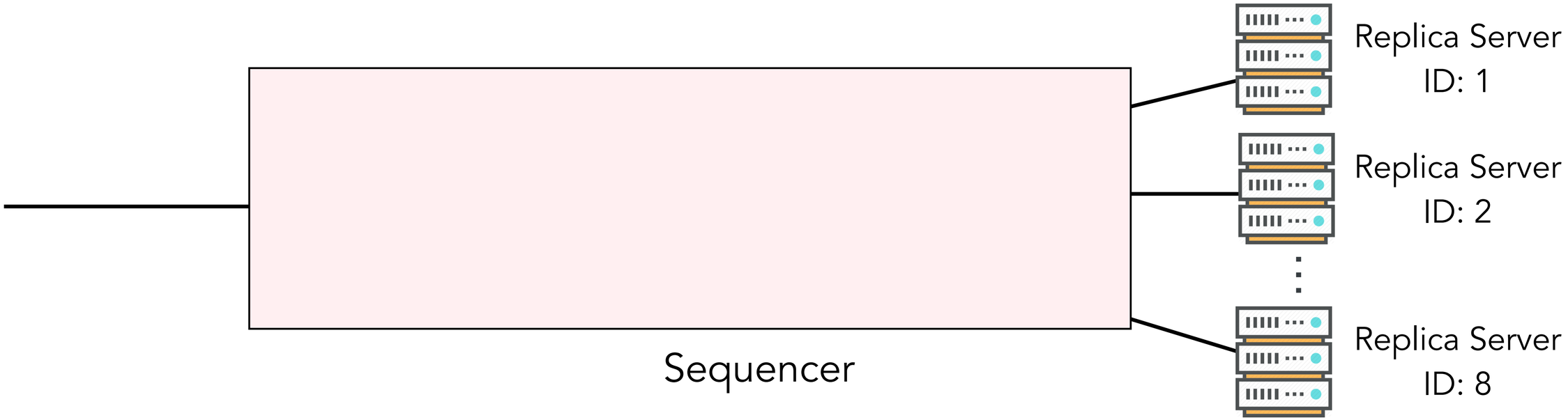
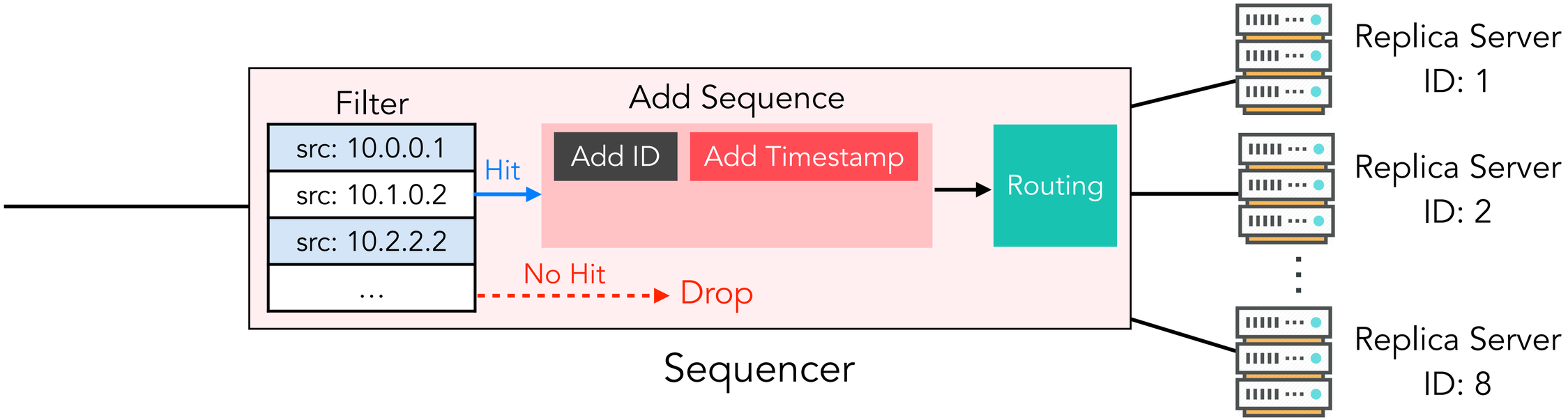


Running example: A network sequencer

Linearizing the transactions for consensus protocols such as Paxos



Add sequence header to selected flows and drop others

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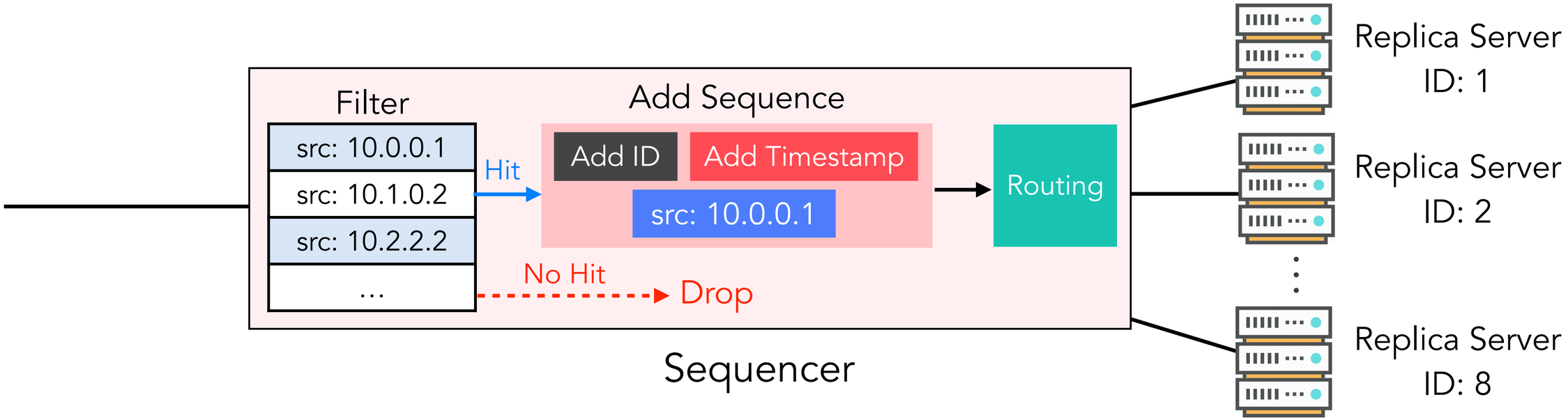

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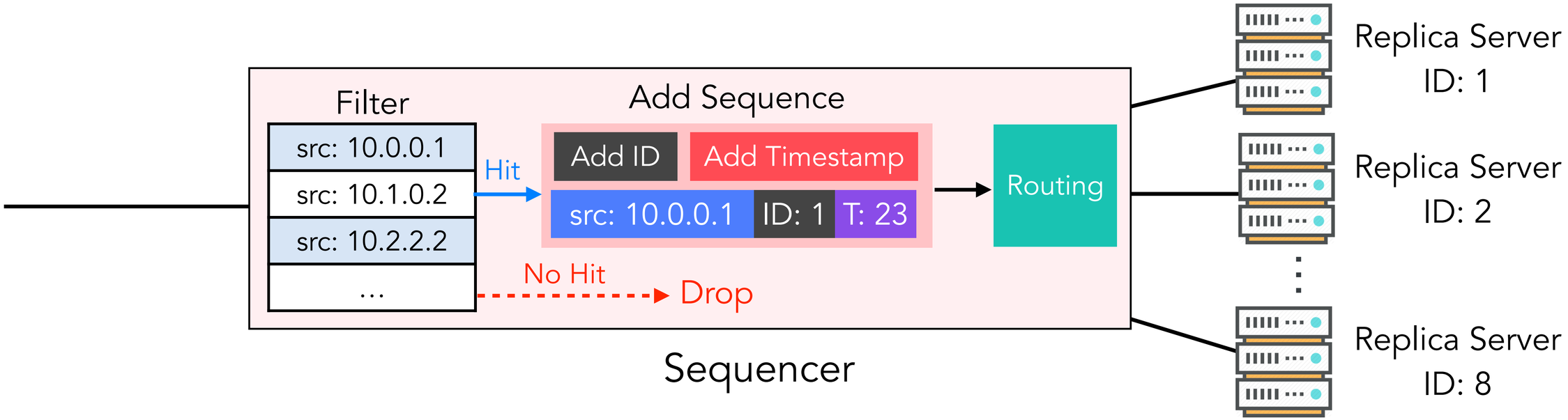

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Problem 1: Portability

Low level, chip-specific languages

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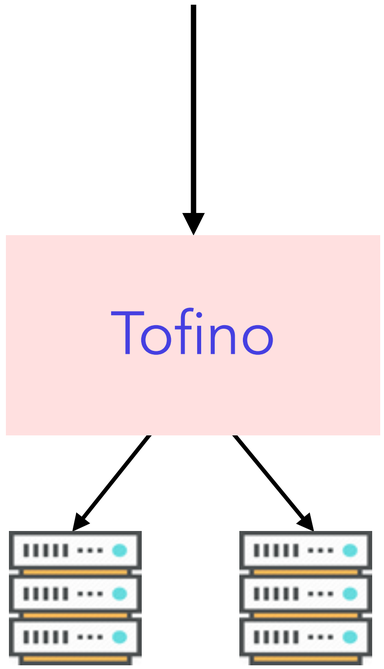

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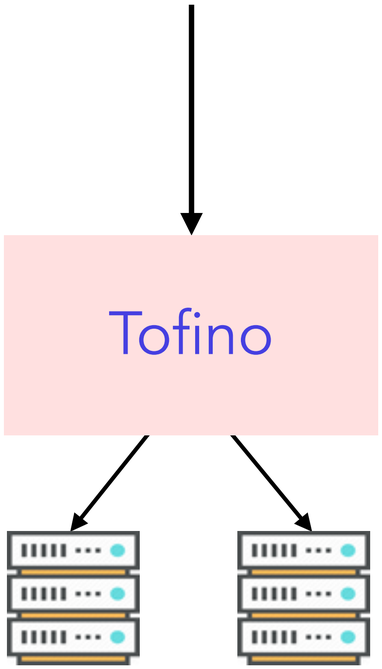


```
// P4_14
action a_shift_switch_id(server_id) {
    shift_left(sequence.seq, server_id, 28);
}
table shift_switch_id {
    reads {
        ipv4.src_ip: exact;
    }
    actions {
        a_shift_switch_id;
    }
}
action a_and_timestamp() {
    bit_and(ig_ts, ig_ts, 0x0FFFFFFF);
}
table and_timestamp {
    actions {
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    }
    default_action: a_and_timestamp();
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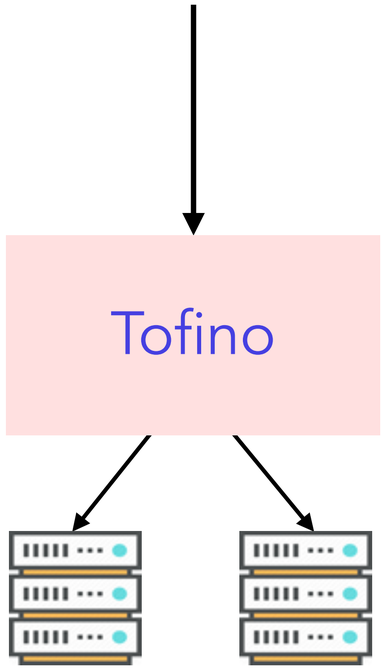

Add ID

Add Timestamp

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add_header(sequence);
sequence.seq = (server_id << 28) & (ig_ts & 0x0FFFFFFF);
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Chip Vendors

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Cannot program across switches

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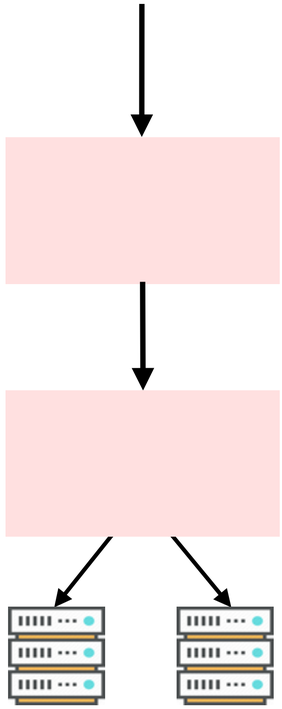

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Cannot program across switches

Aggregation
1000 entries

Top of Rack
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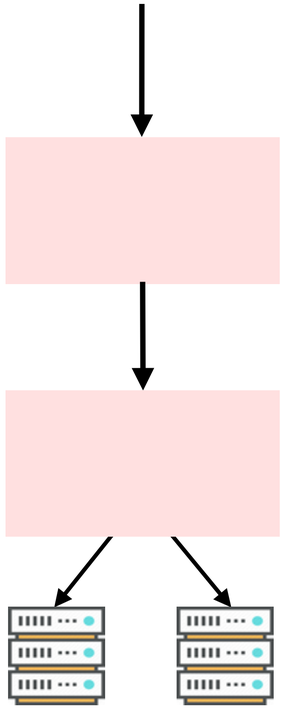

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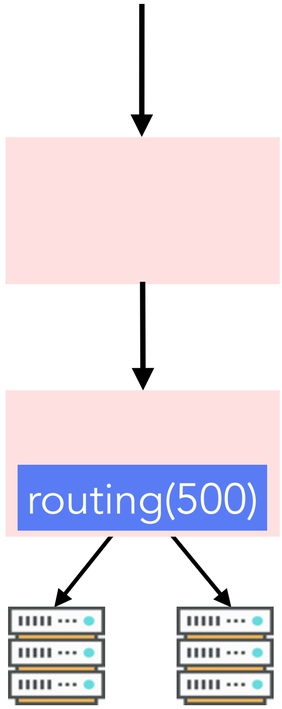

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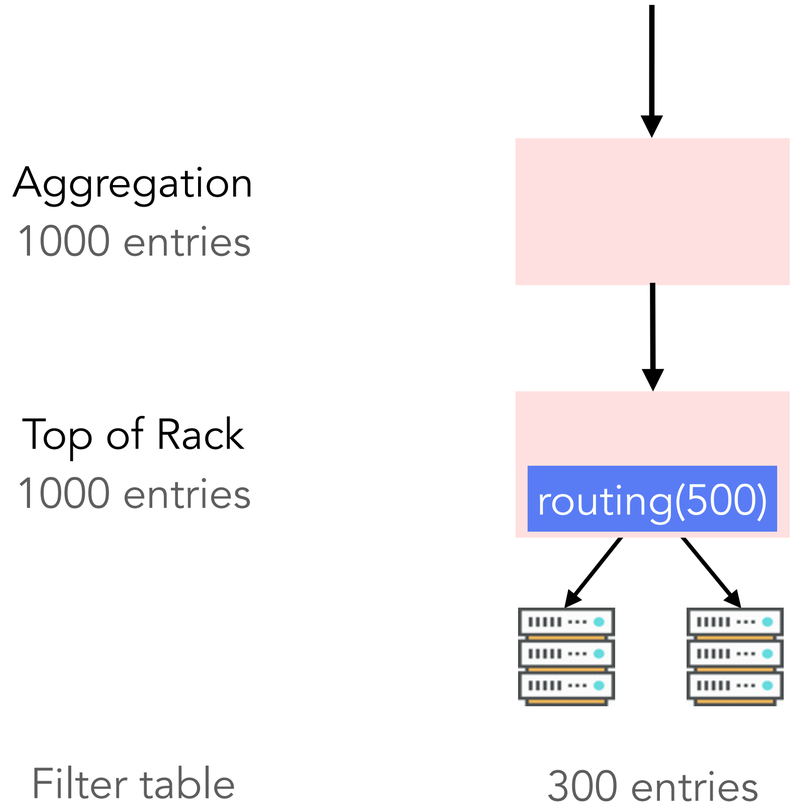

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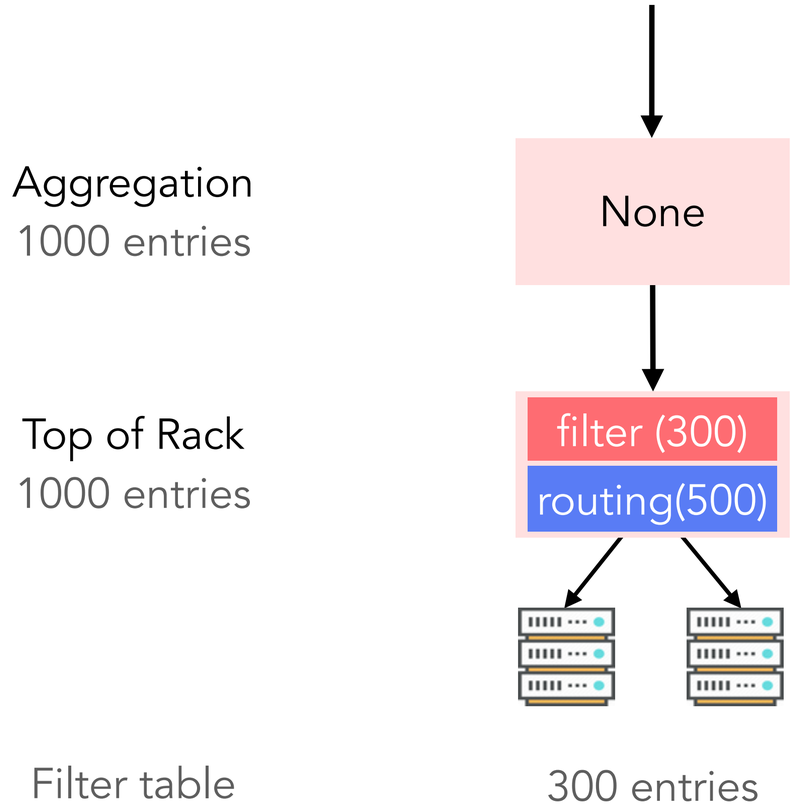

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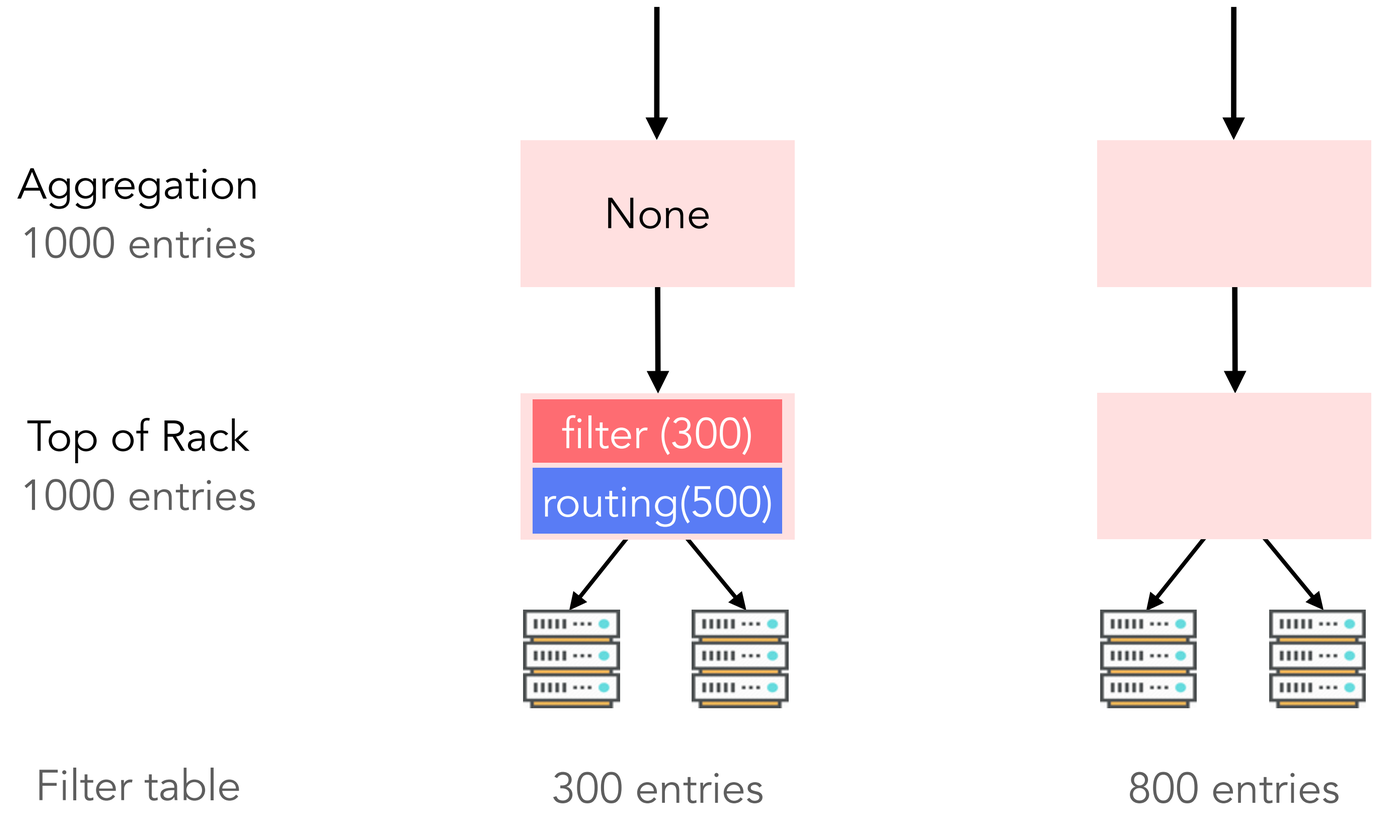

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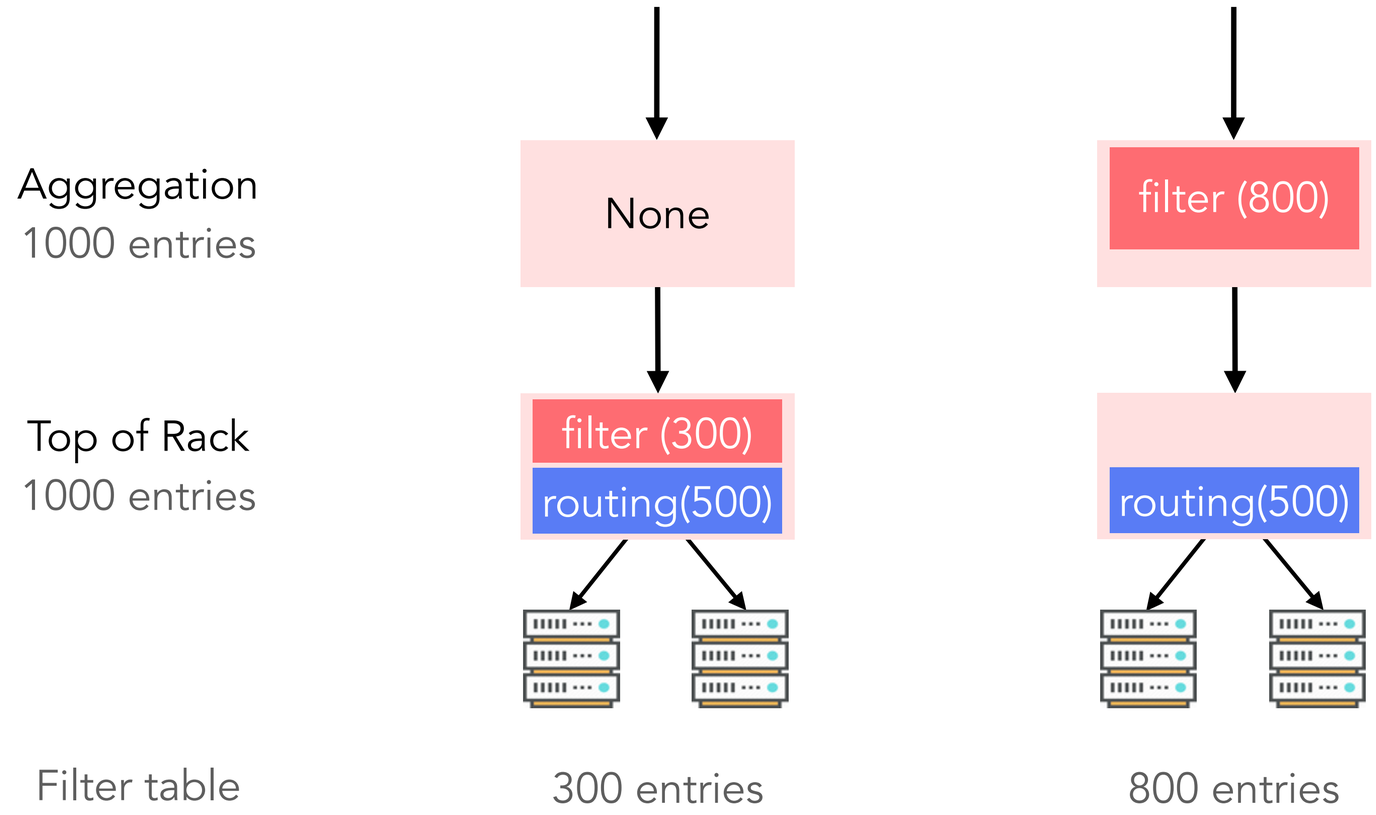

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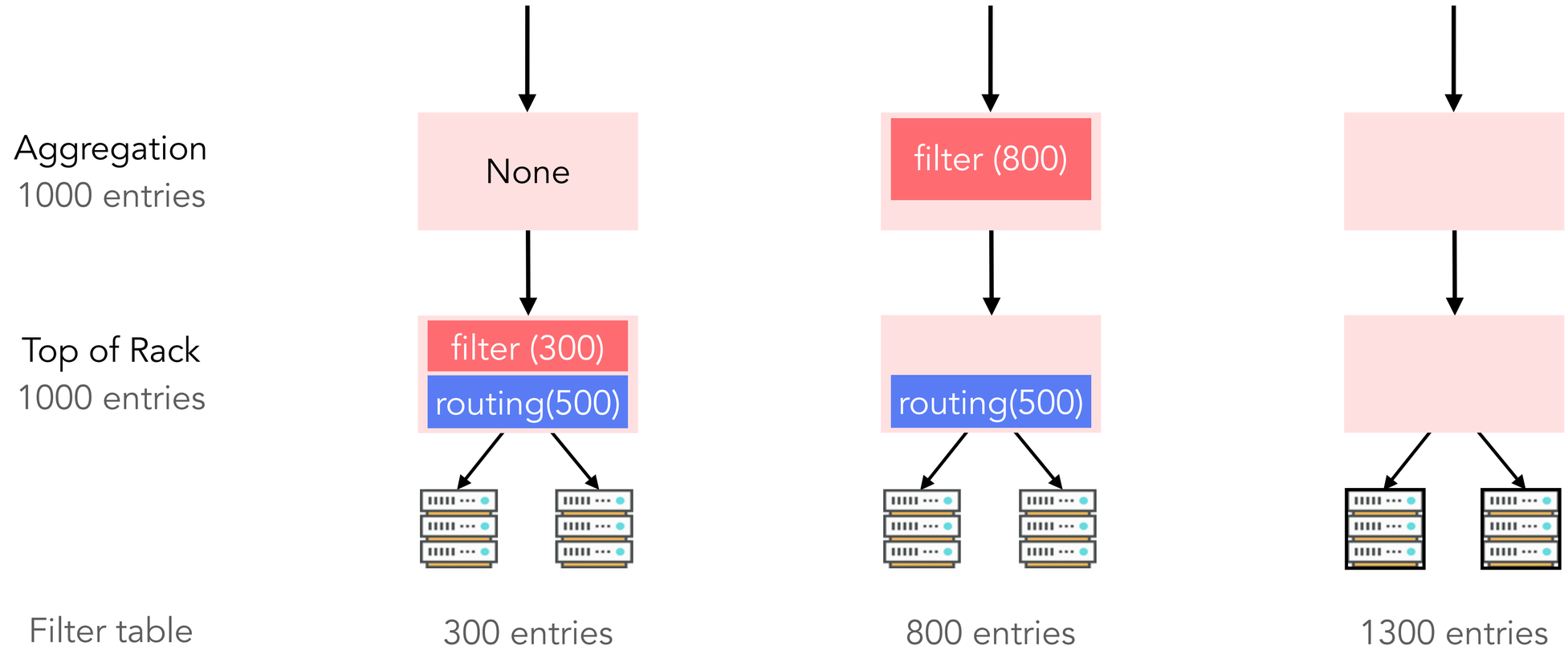

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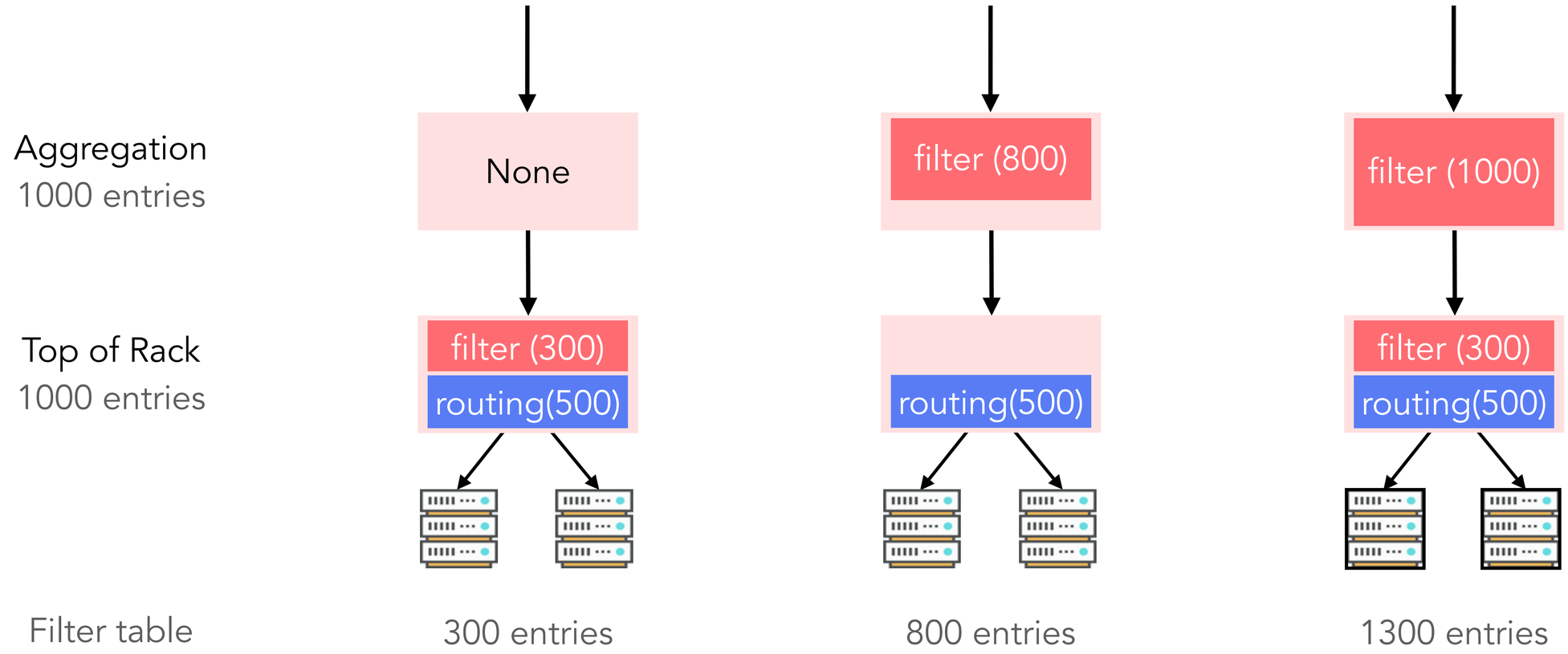

Problem 3: Composition

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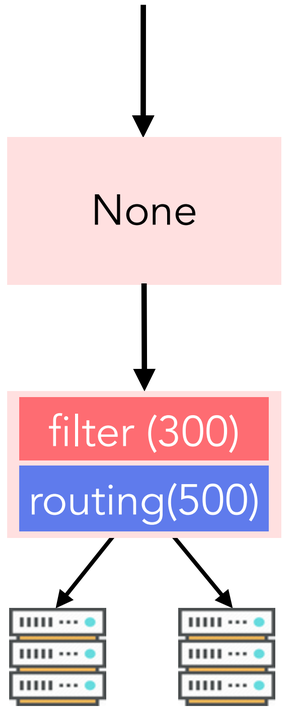

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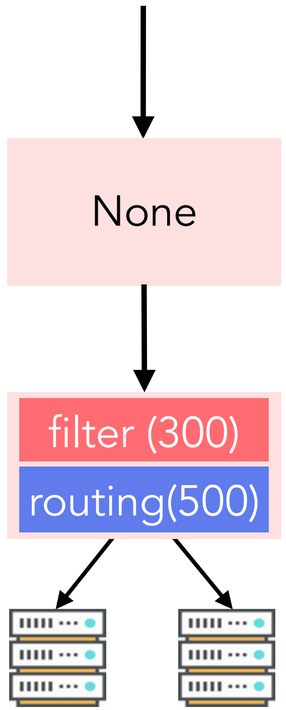

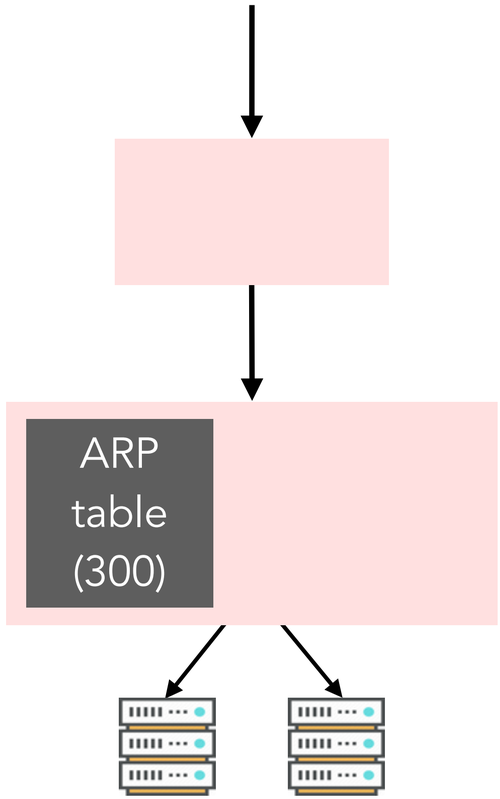

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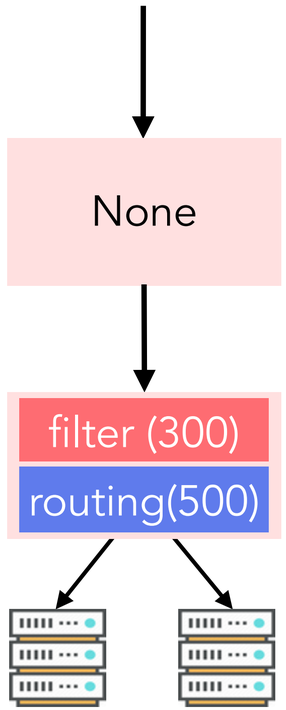

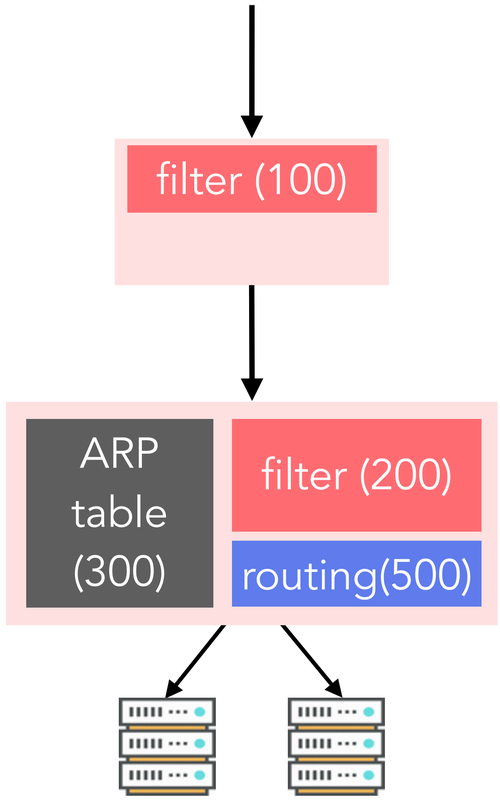

Data plane programming is still at an early stage

Portability

Migrate program across switches

Different languages
Different architectures
Different ASIC models

Extensibility

Distribute program across multiple switches

Different roles (In-band network telemetry)
Expand memory or computation (Sequencer)

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Fit multiple programs into one switch

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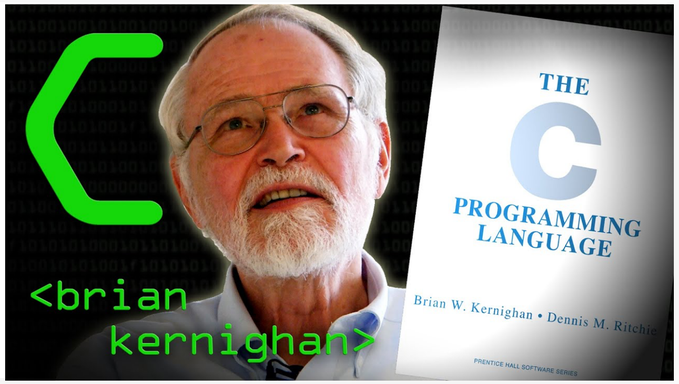

Lyra: A high-level data plane language & compiler

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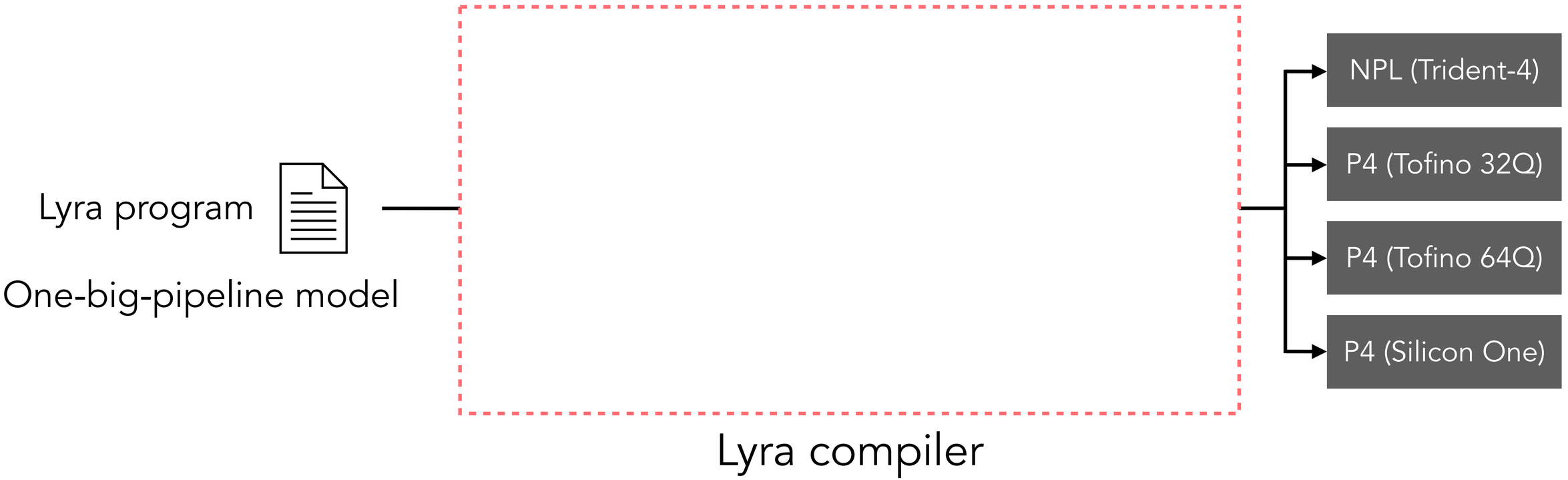
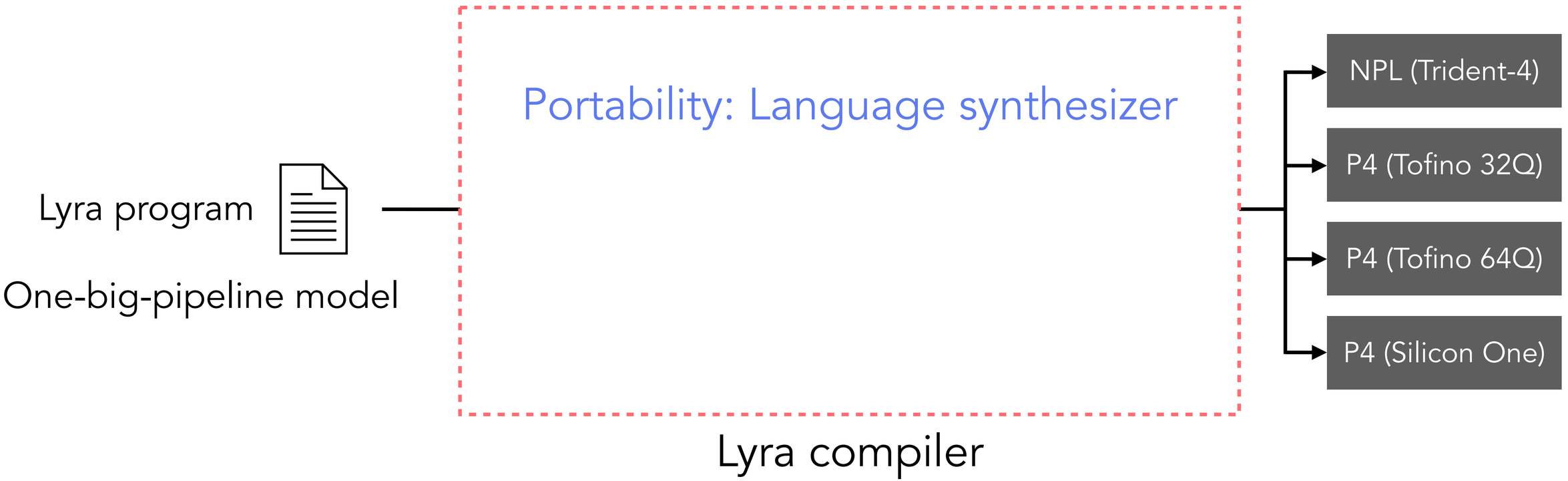
Lyra program 

One-big-pipeline model

Lyra: A high-level data plane language & compiler



Lyra: A high-level data plane language & compiler



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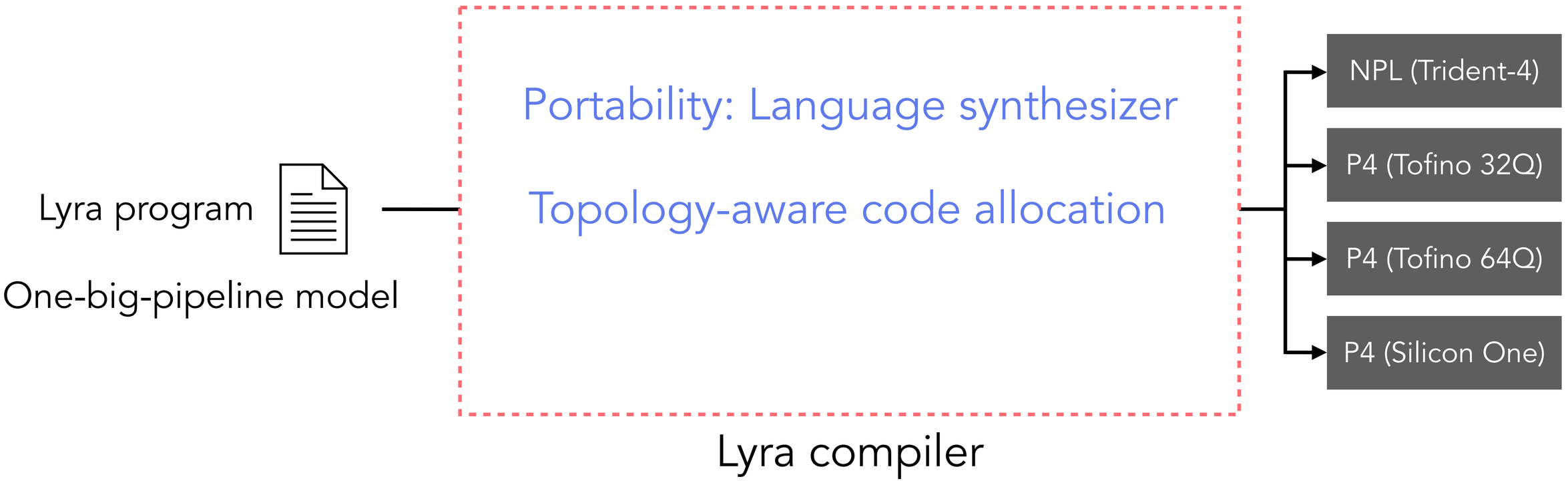

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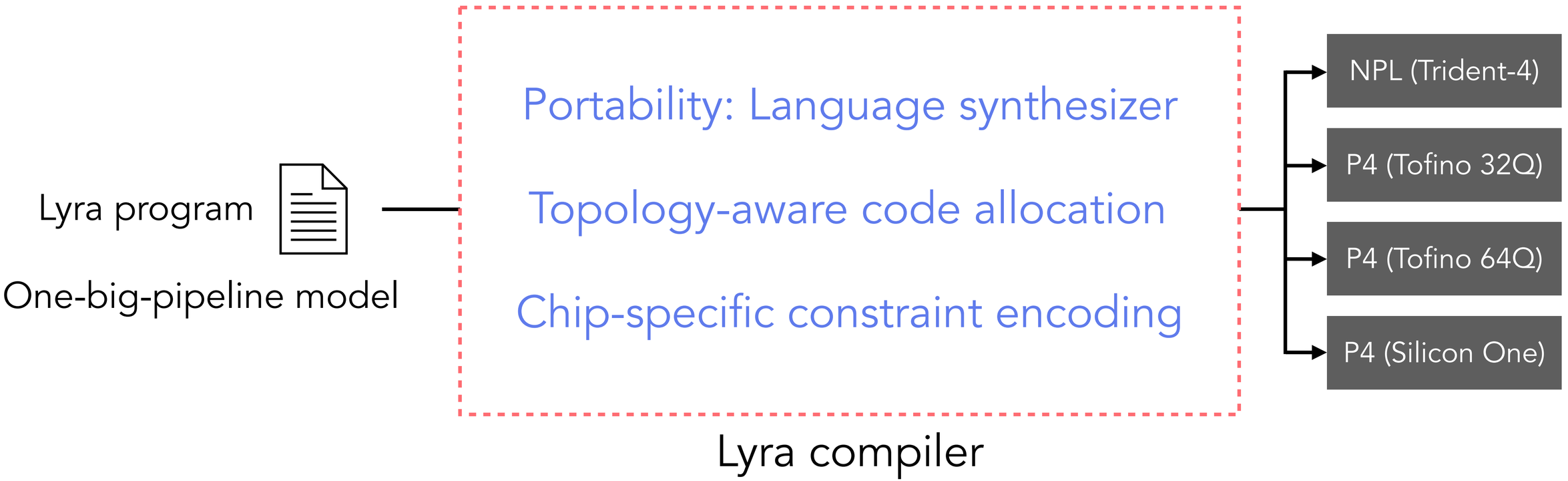

Lyra language: One-big-pipeline model

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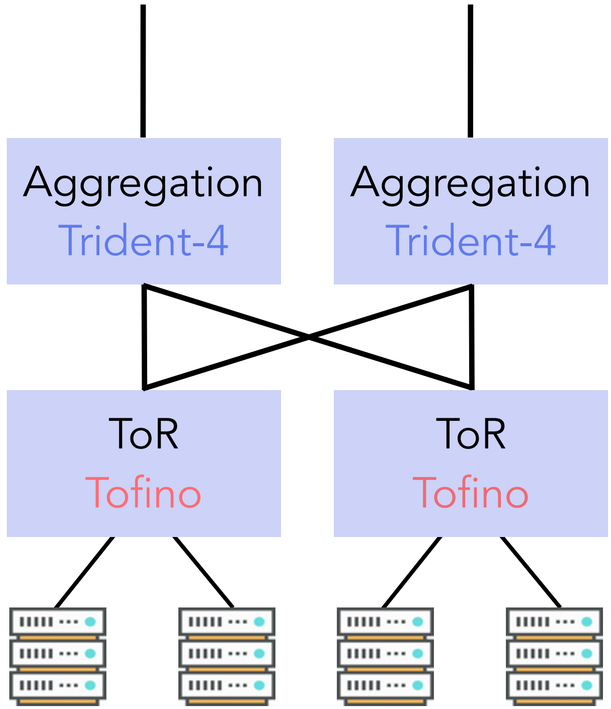

Per-switch model

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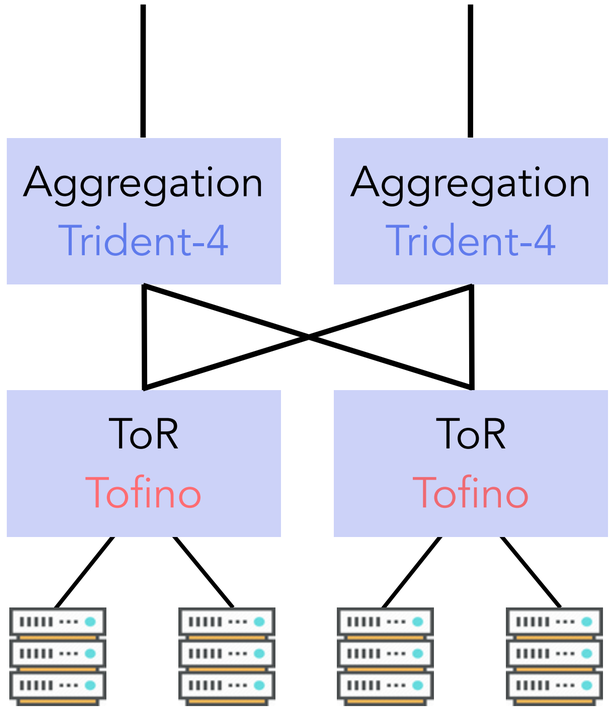

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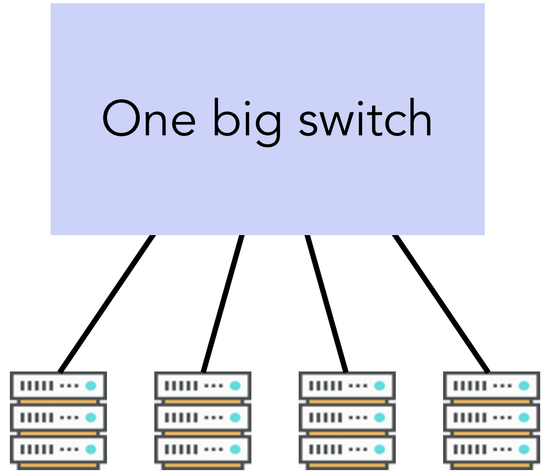

One-big-switch model

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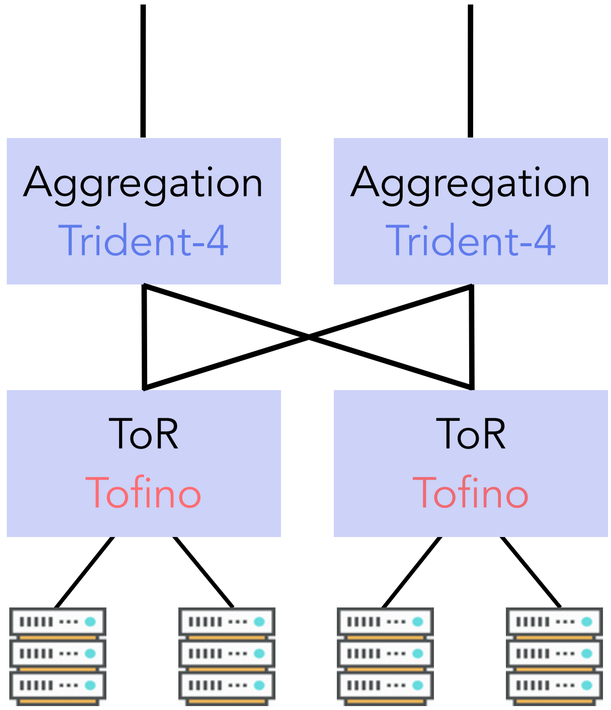

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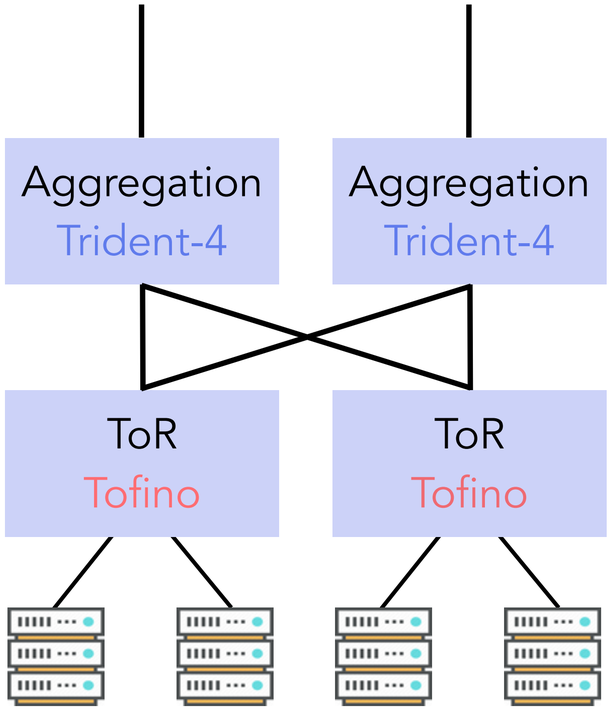

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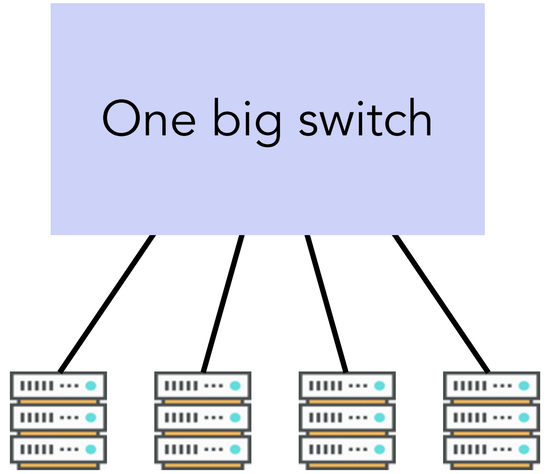

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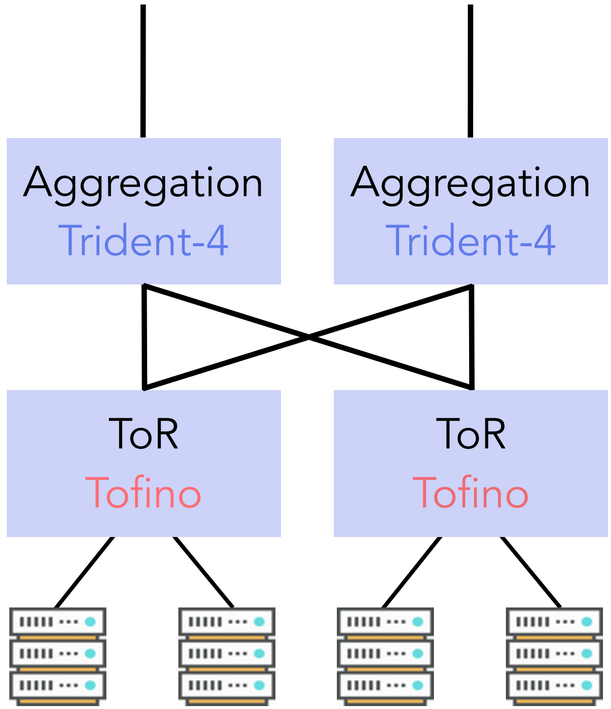

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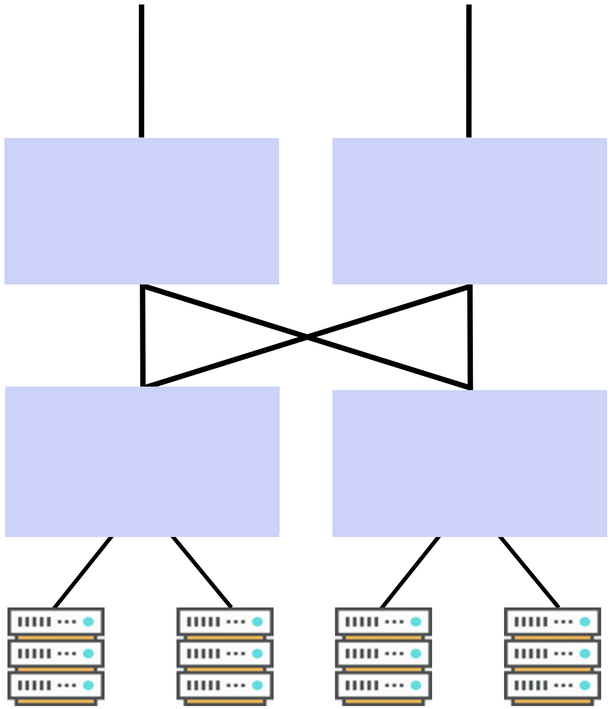

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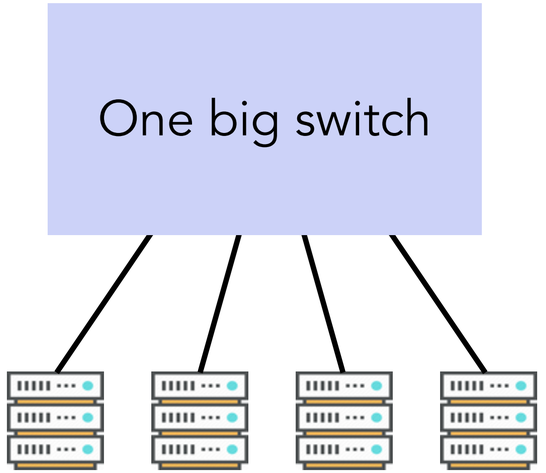

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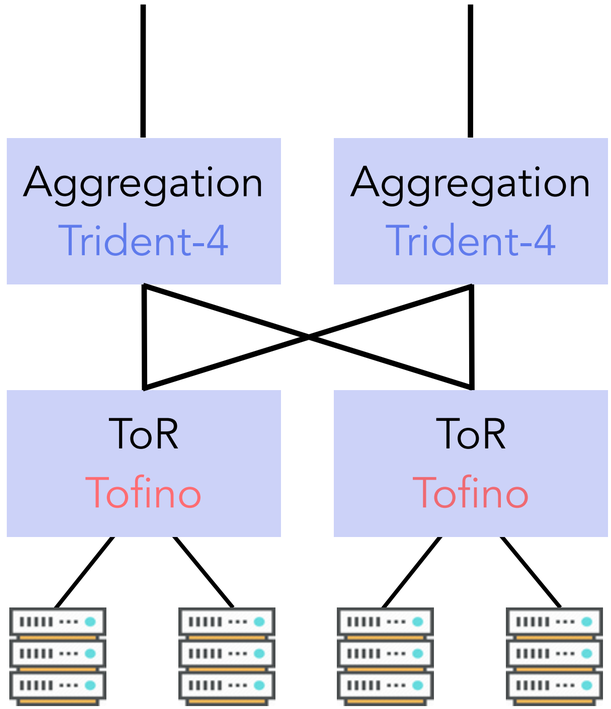

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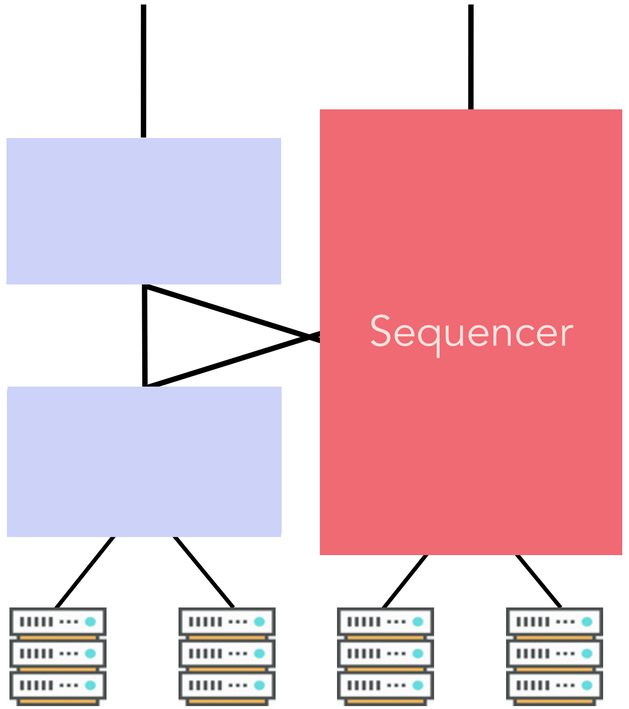
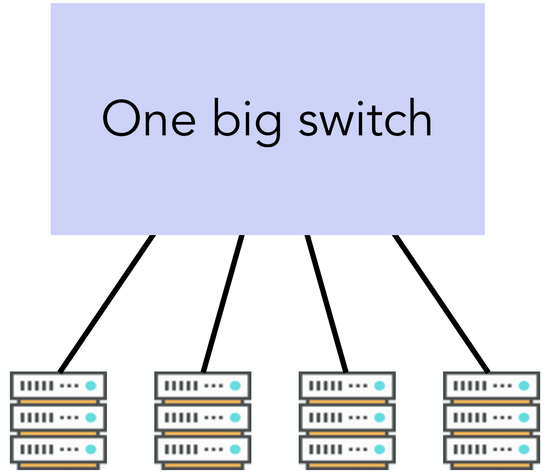
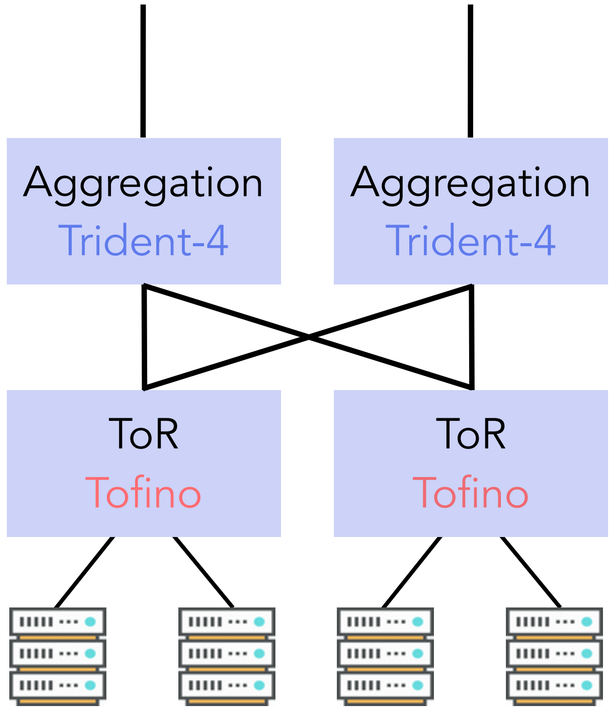


One-big-pipeline model

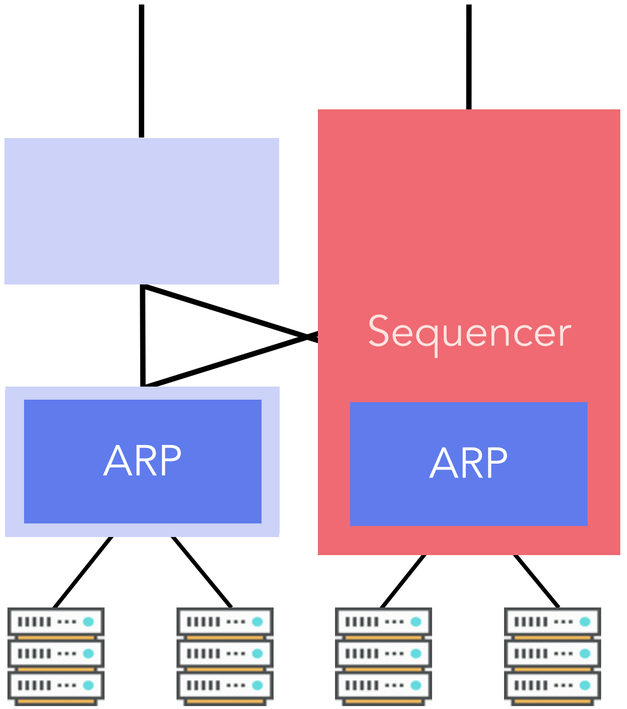


One-big-switch model

Lyra language: One-big-pipeline model



Per-switch model



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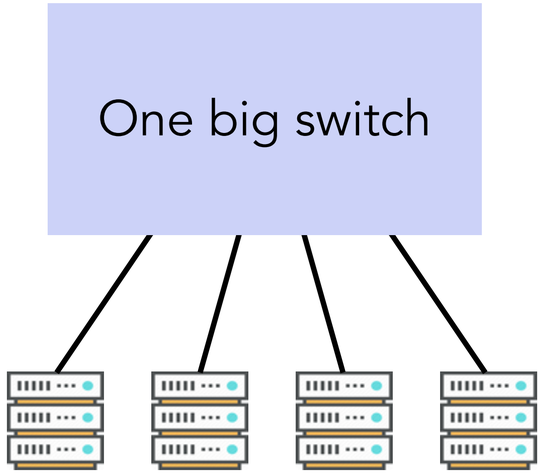

One-big-switch model

Lyra language: Program

Alibaba Cloud
Worldwide Cloud Services Partner

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pipeline[SEQ] {sequencer};

algorithm sequencer {
    add_sequence();
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func add_sequence() {
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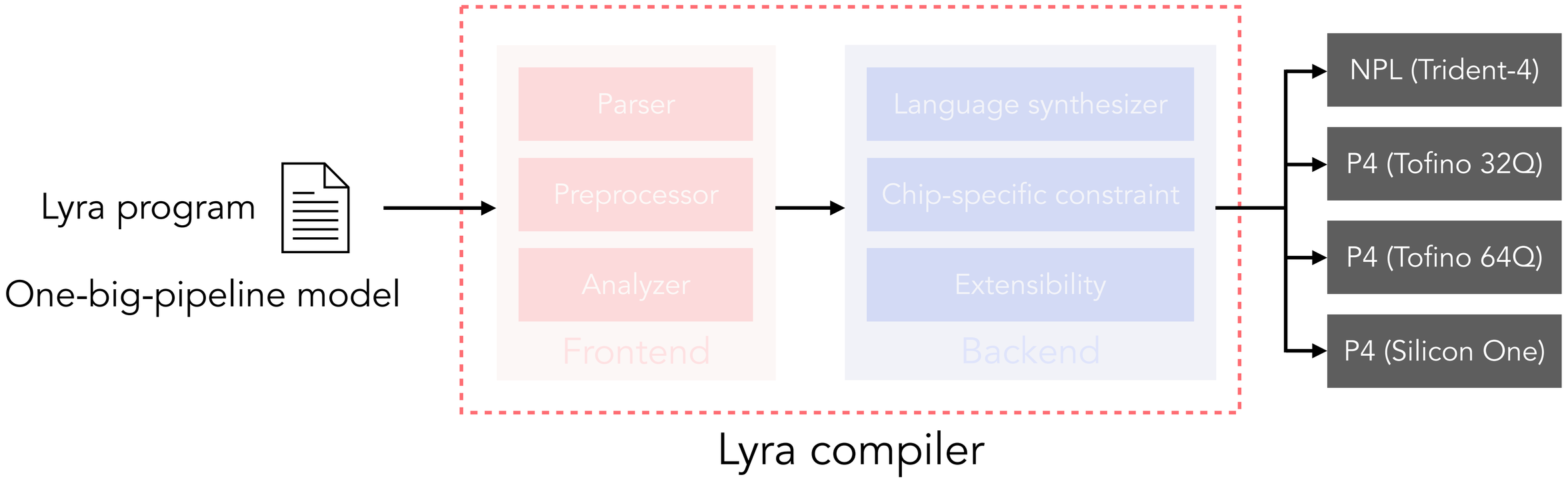
Lyra: A high-level data plane language & compiler

Alibaba Cloud
Worldwide Cloud Services Partner



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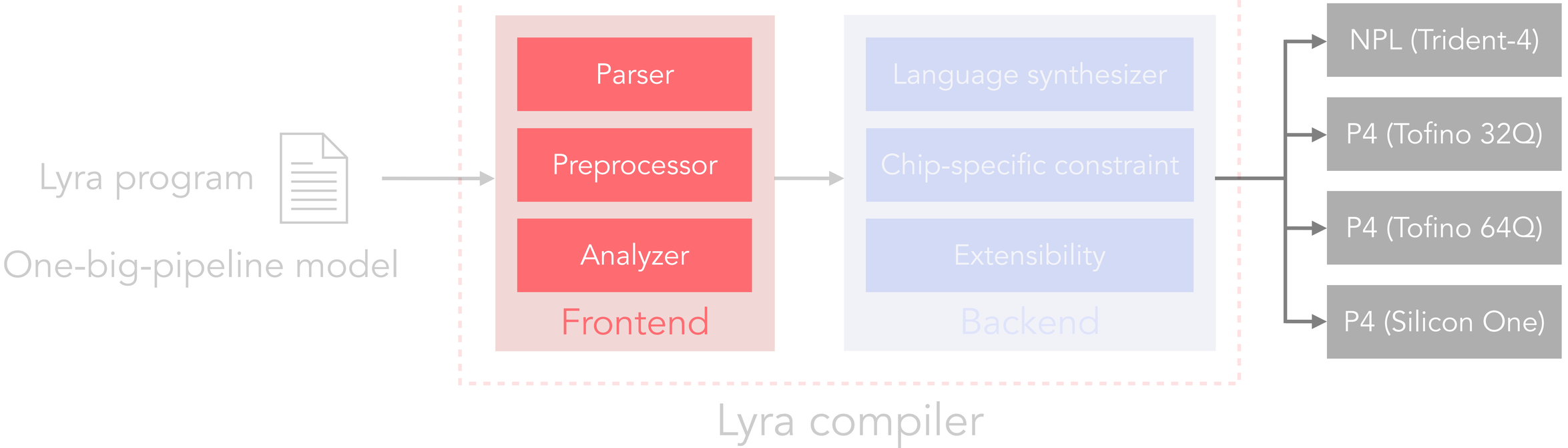

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Lyra program

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Intermediate representation

One big pipeline model

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One big pipeline model

No complex statements

No branches

Has statement dependencies

Lyra: A high-level data plane language & compiler

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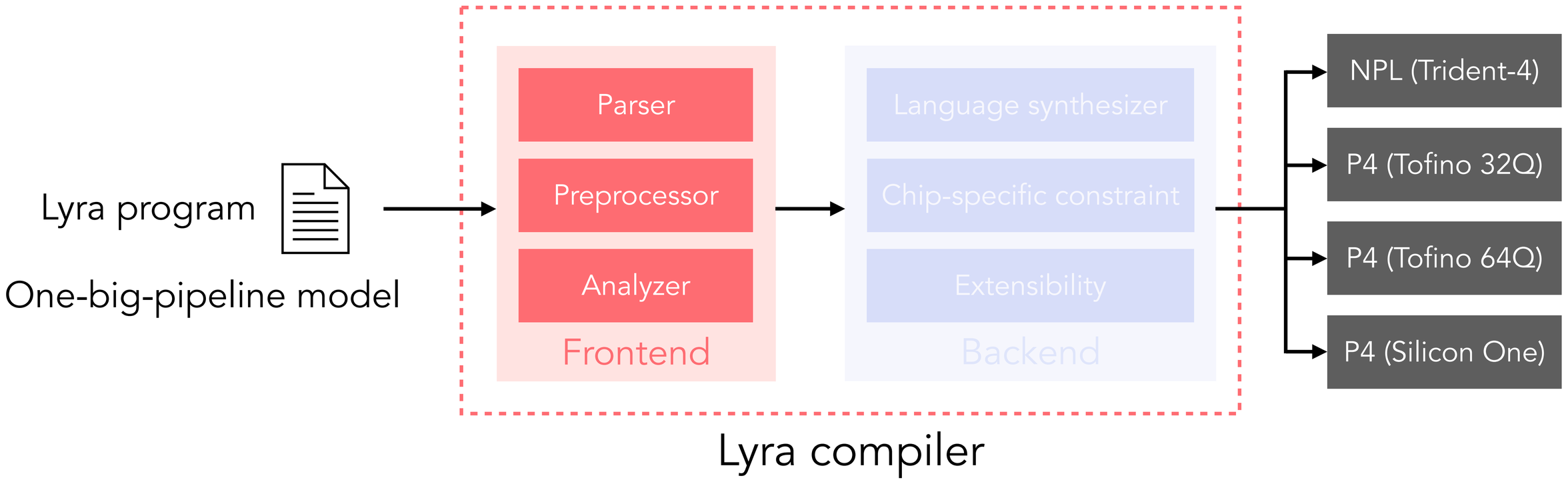
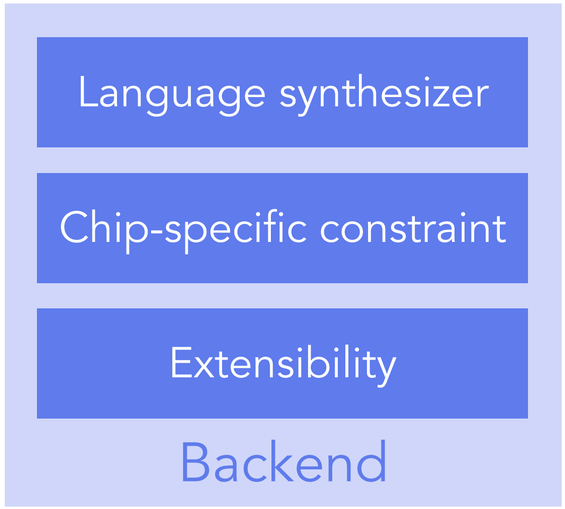
Worldwide Cloud Services Partner



Lyra: A high-level data plane language & compiler



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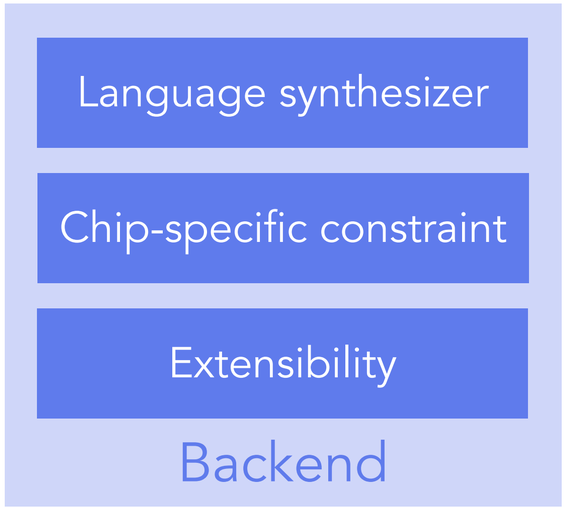

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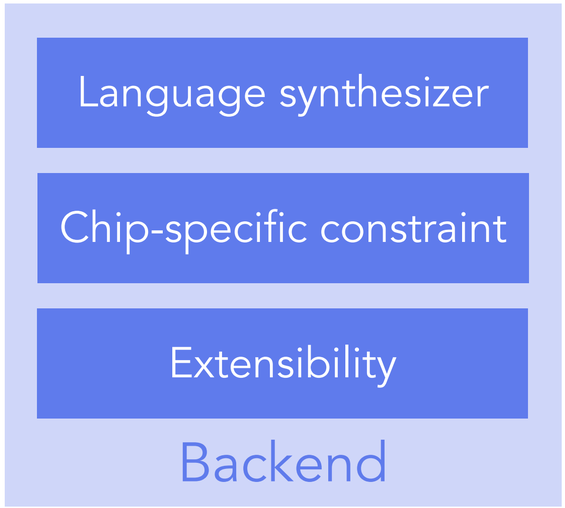
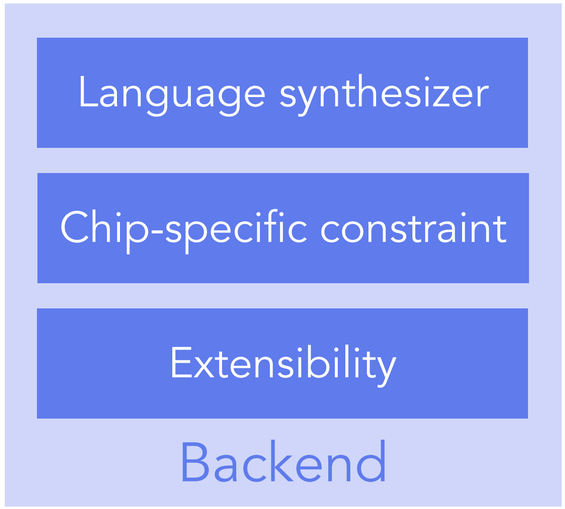


Portability I Compile Lyra into structured low level languages

Lyra: A high-level data plane language & compiler

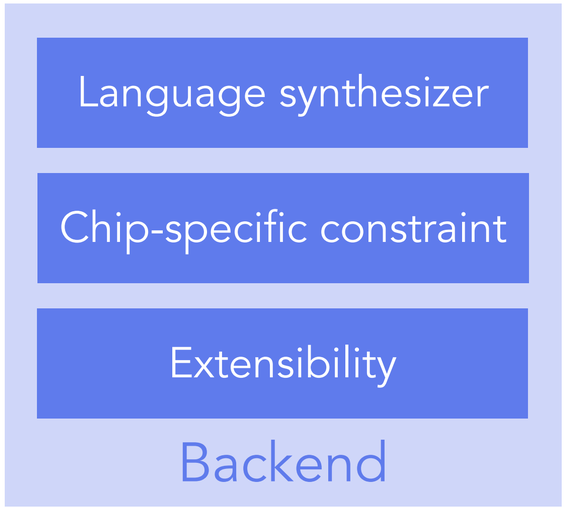


Portability | Compile Lyra into structured low level languages

Composition | Checks whether the program can fit into the switch

Lyra: A high-level data plane language & compiler

Alibaba Cloud
Worldwide Cloud Services Partner



Portability | Compile Lyra into structured low level languages

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Lyra: A high-level data plane language & compiler

Alibaba Cloud
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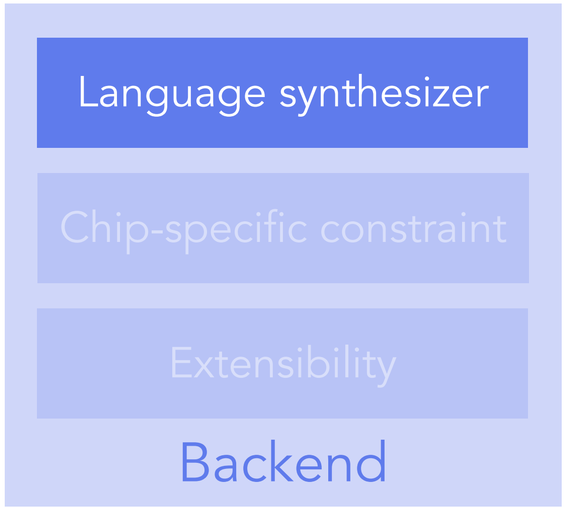

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Languages have different programming paradigms

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Table oriented programming

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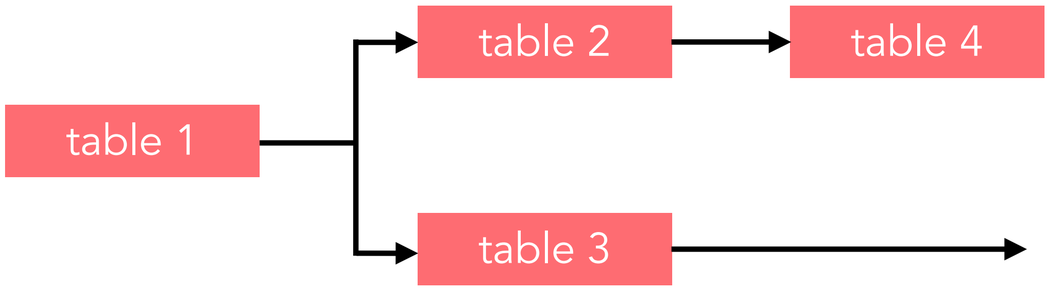
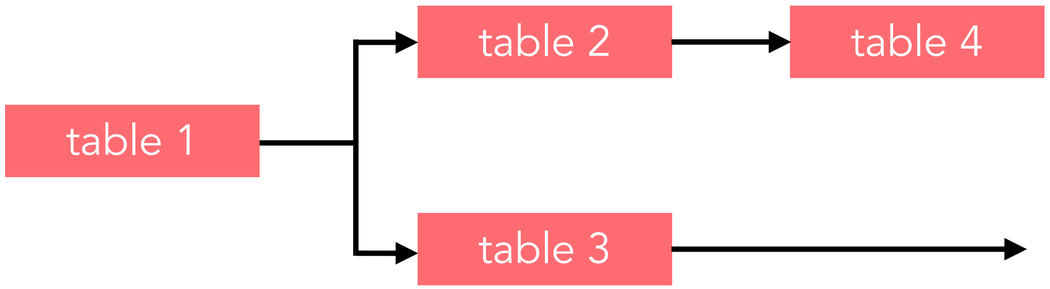


P4 Program

Languages have different programming paradigms

Table oriented programming



P4 Program

Procedural oriented programming

P4 Table

Languages have different programming paradigms

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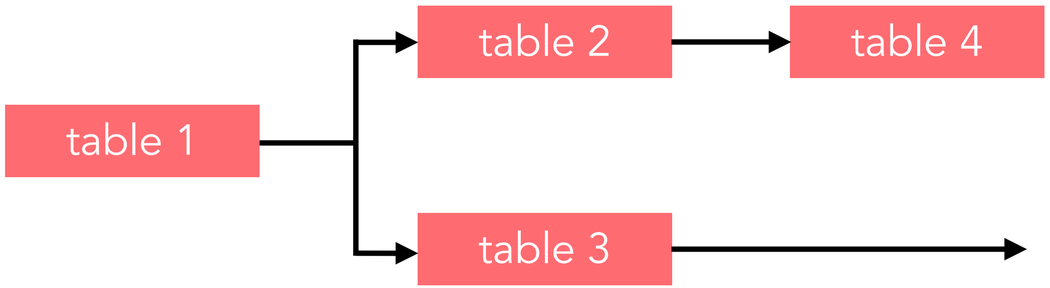

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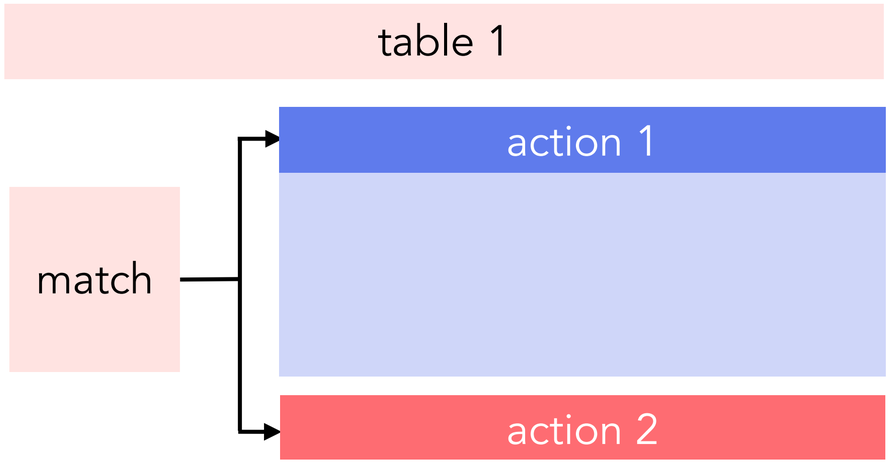

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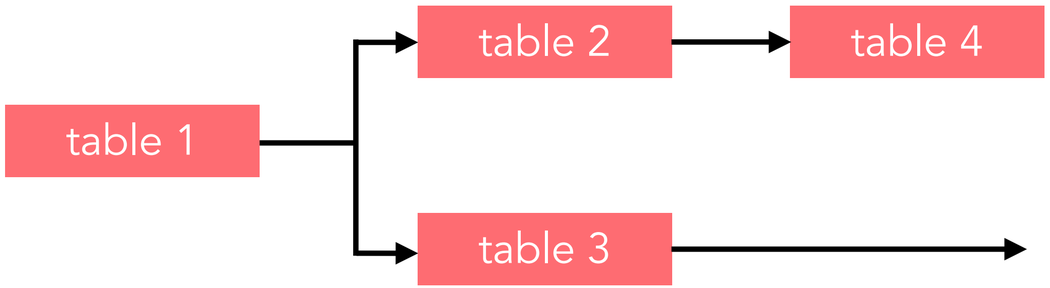

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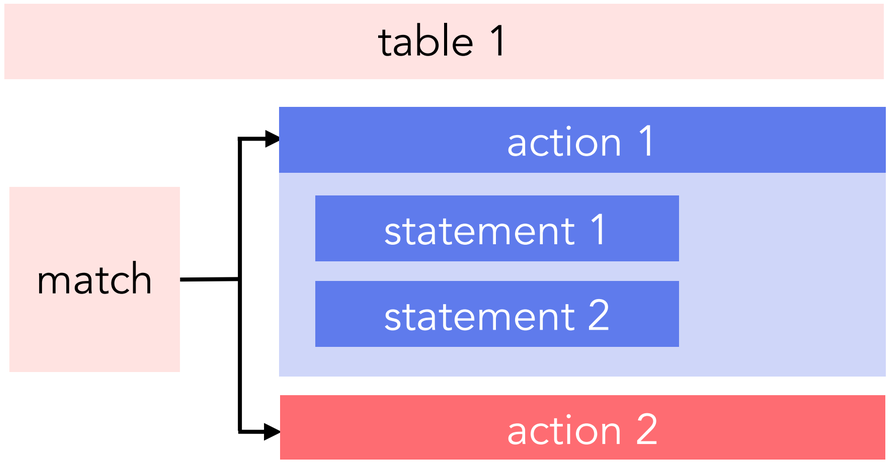

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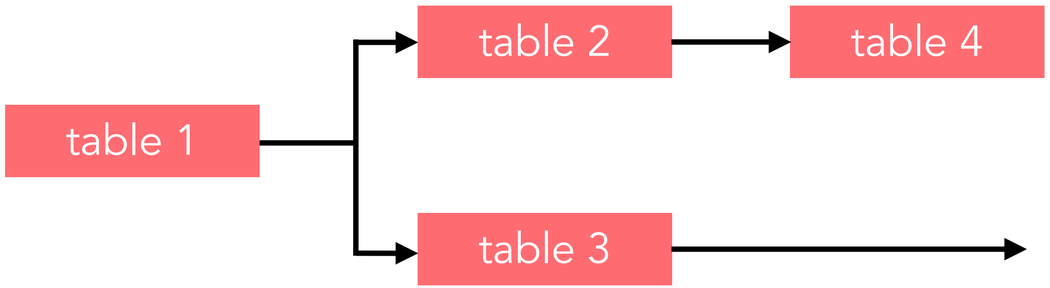

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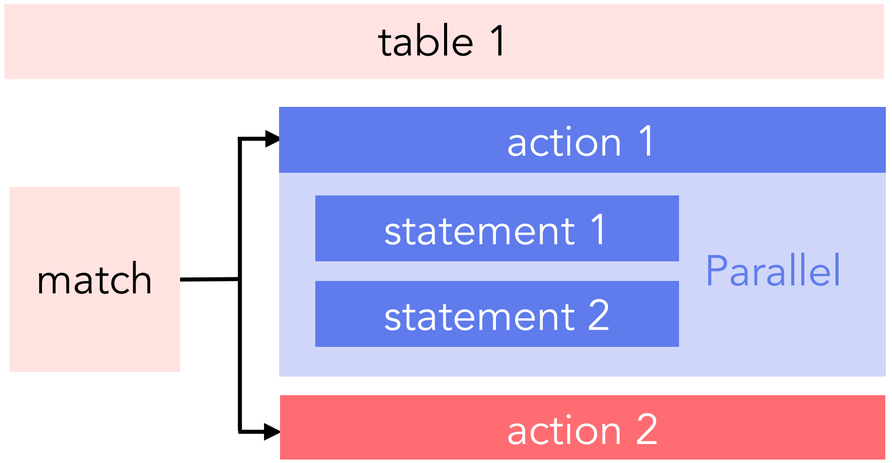

P4 Table

Predicate block

Predicate block

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Worldwide Cloud Services Partner

Group of statements that has the same predicate and no dependency

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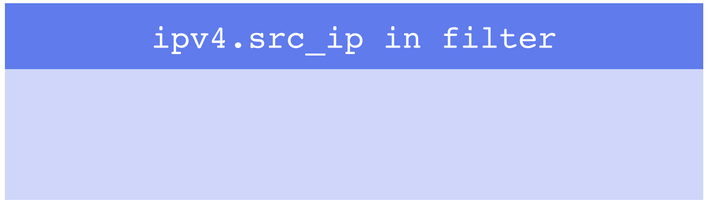

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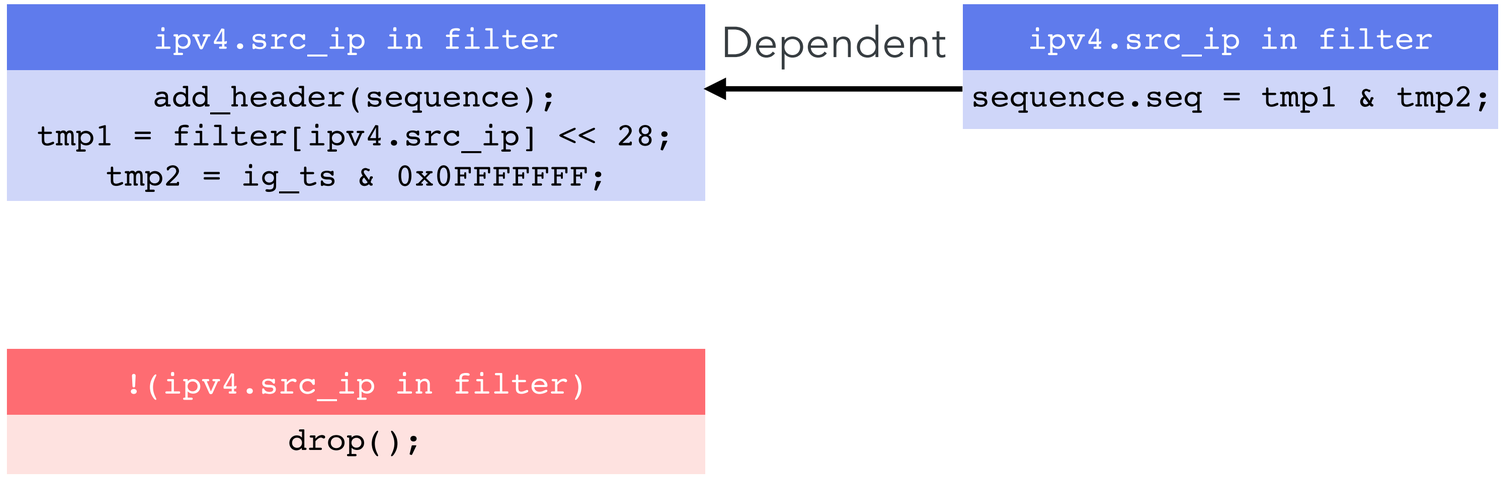
Group of statements that has the same predicate and no dependency

```
p1 = ipv4.src_ip in filter;
     add_header(sequence);
     tmp1 = filter[ipv4.src_ip] << 28;
     tmp2 = ig_ts & 0x0FFFFFFF;
     sequence.seq = tmp1 & tmp2;

p2 = !(ipv4.src_ip in filter);
     drop();
```



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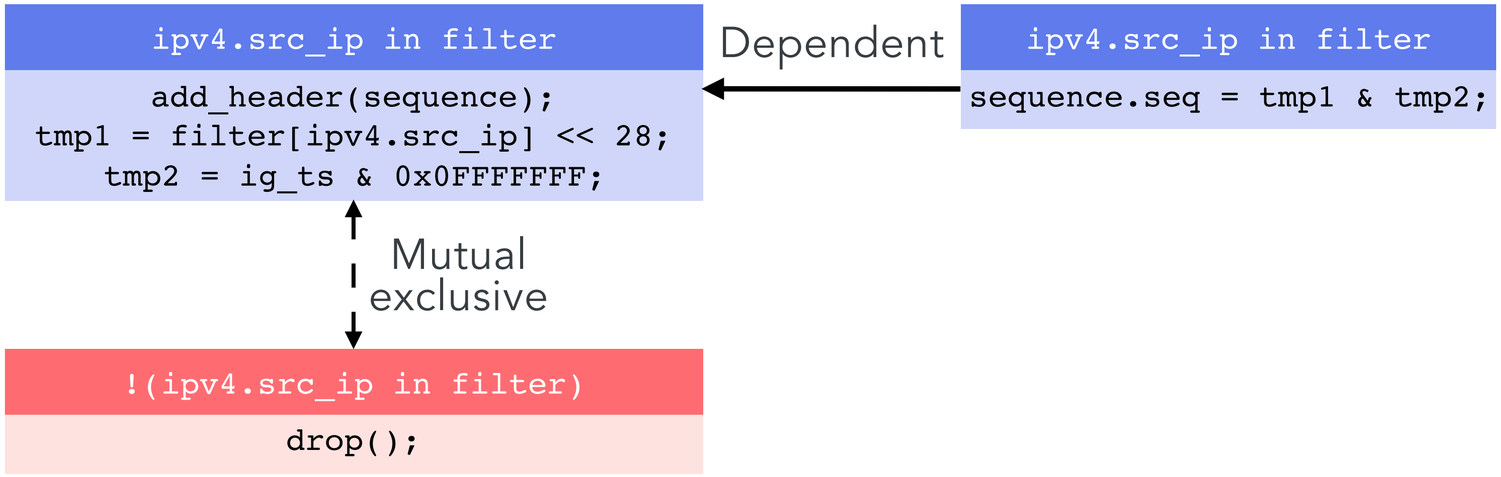

Predicate block

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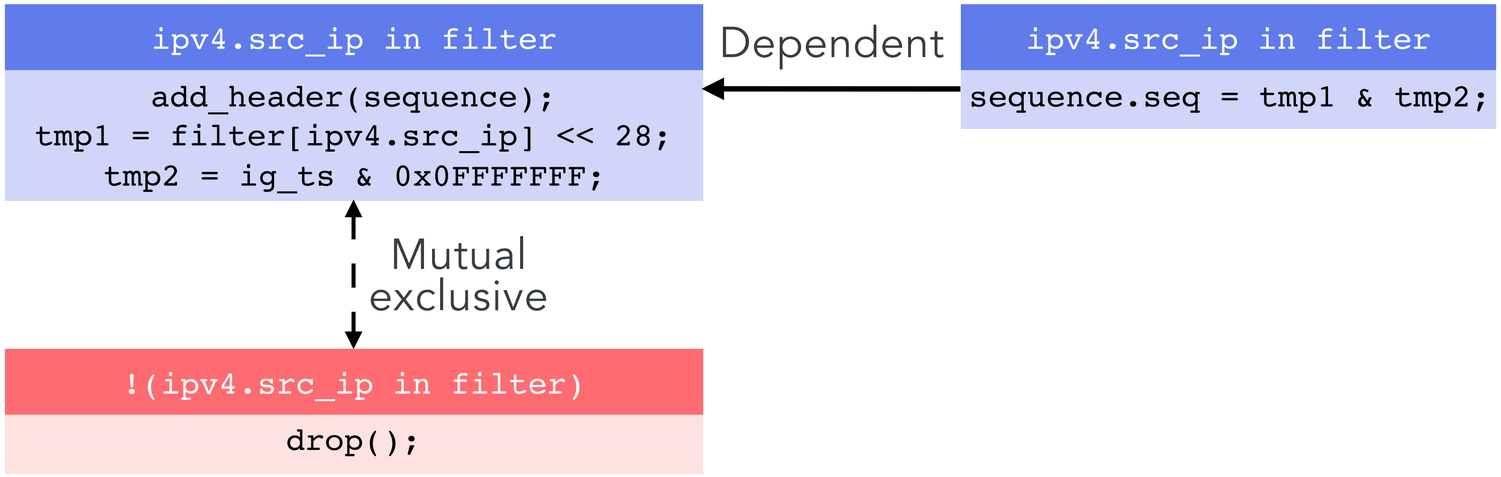

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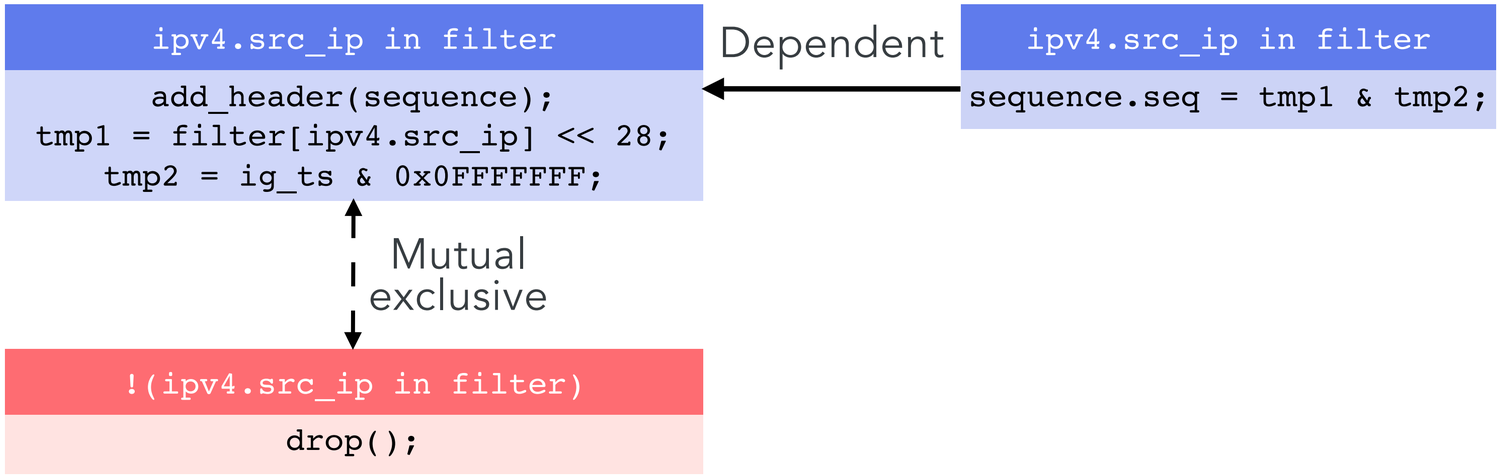

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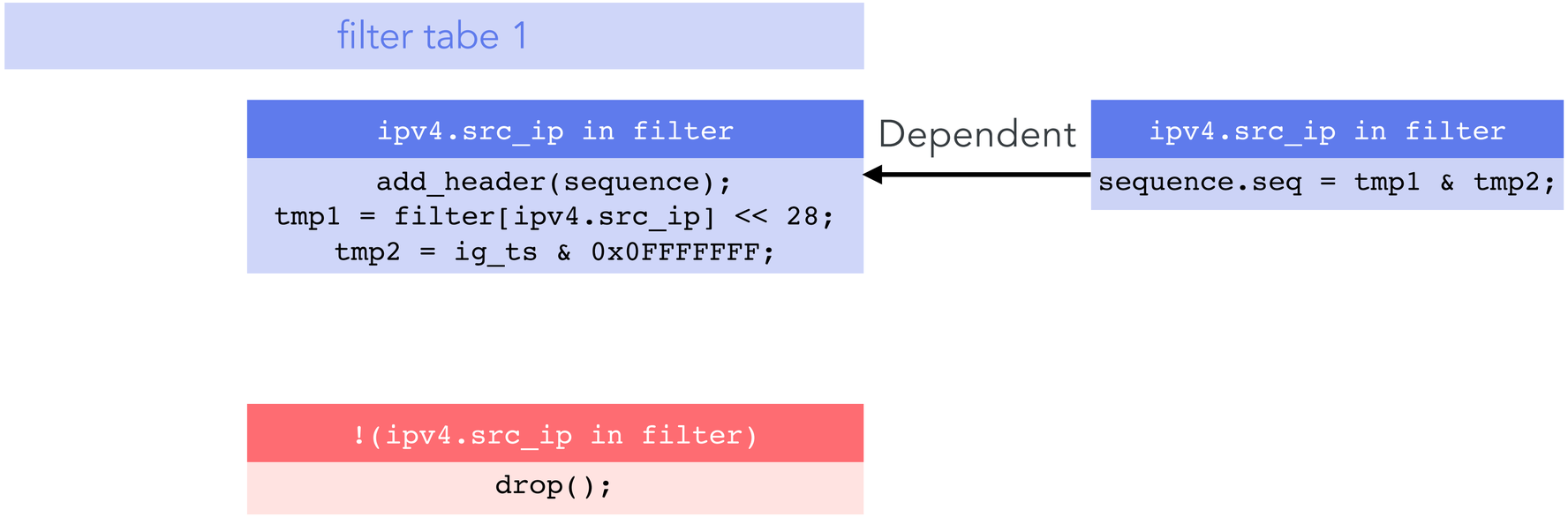

Predicate block

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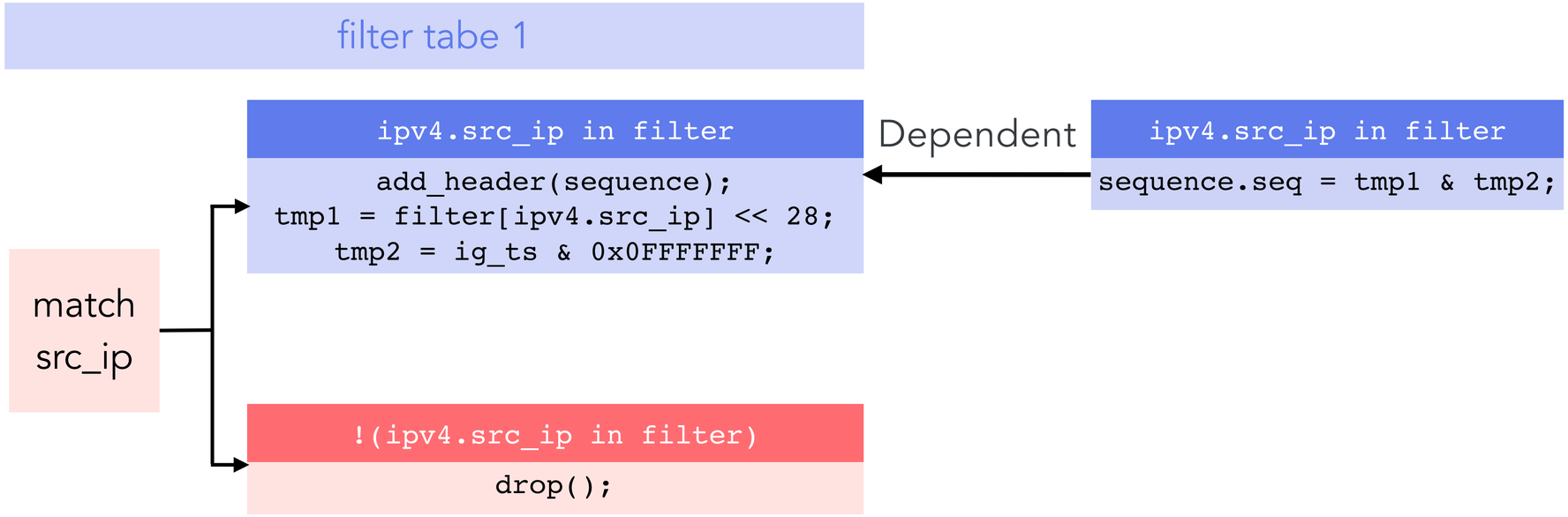

Predicate block

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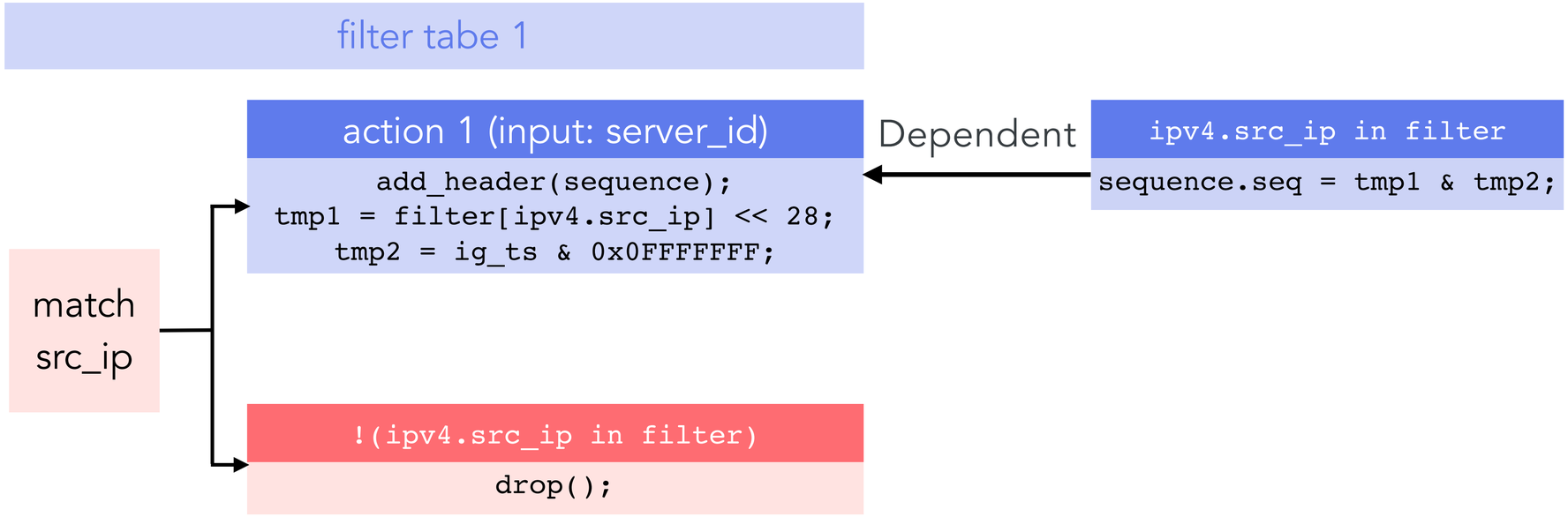

Predicate block

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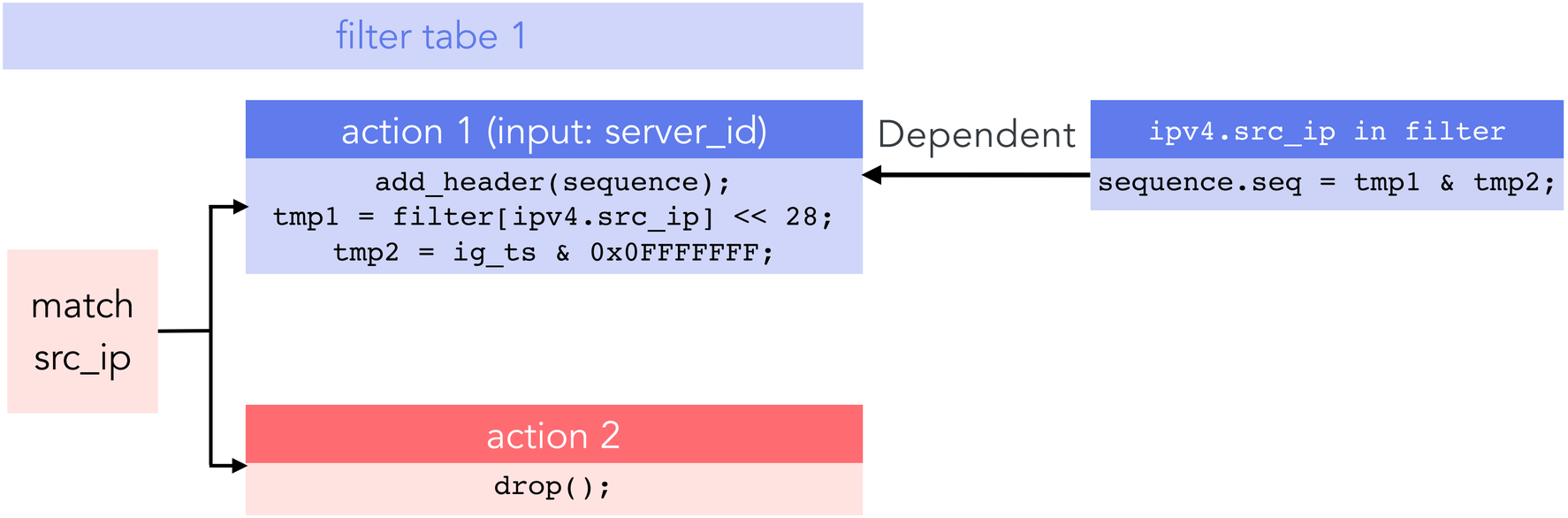

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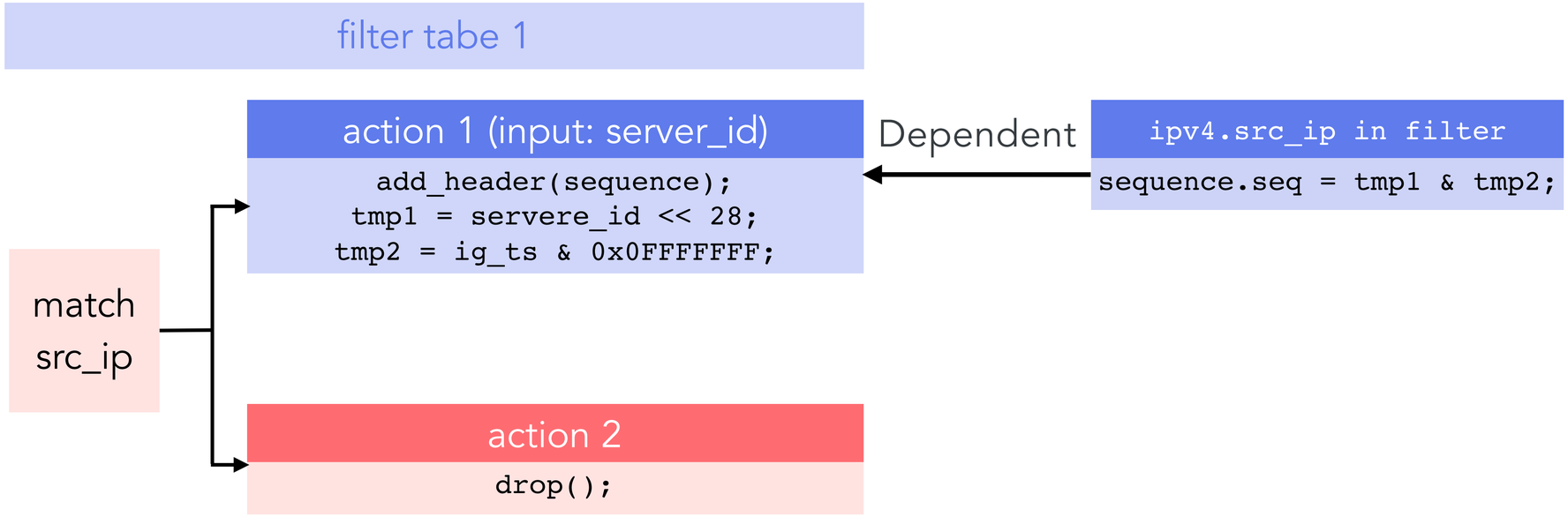

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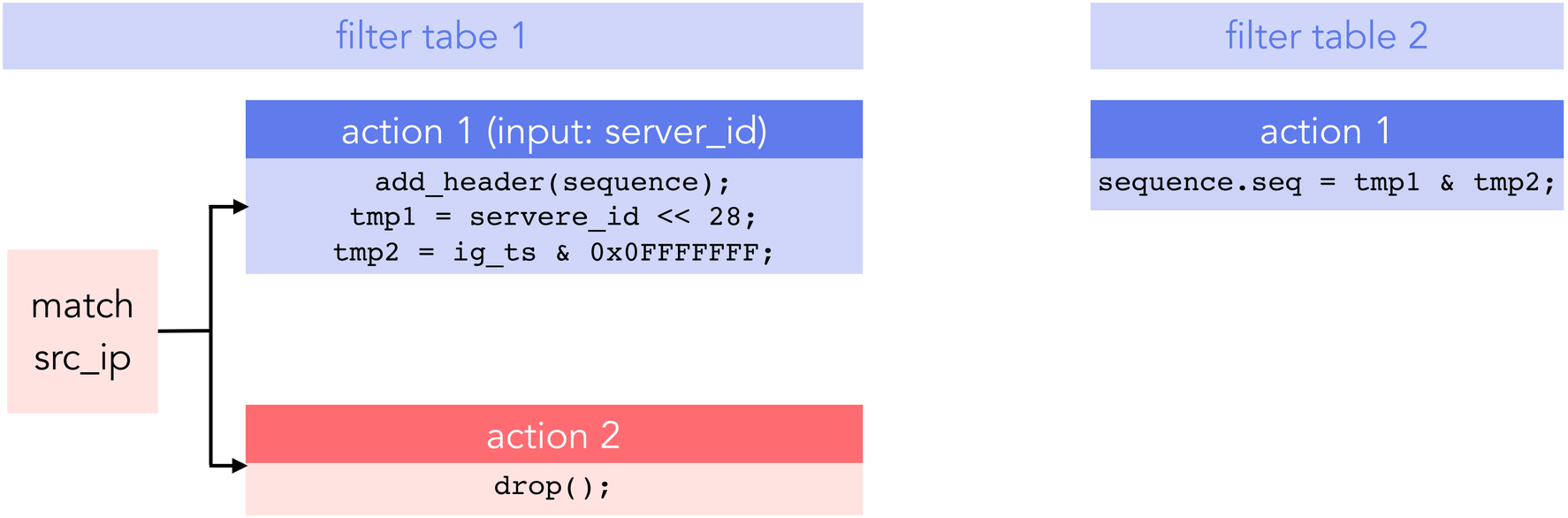

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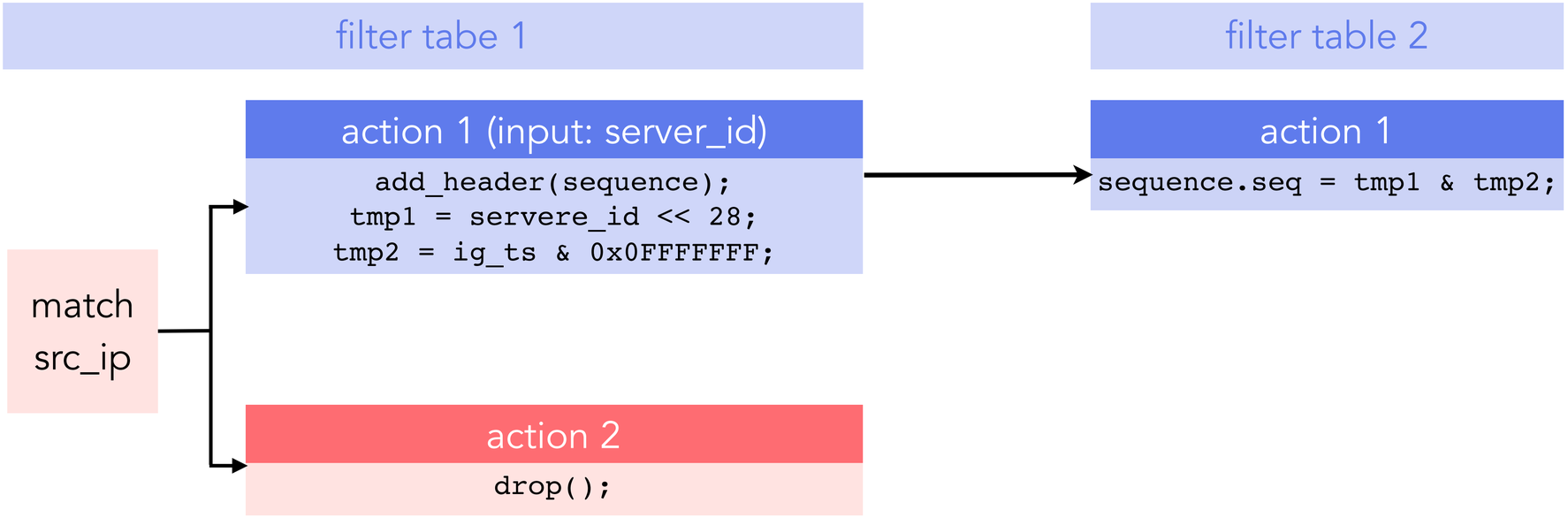
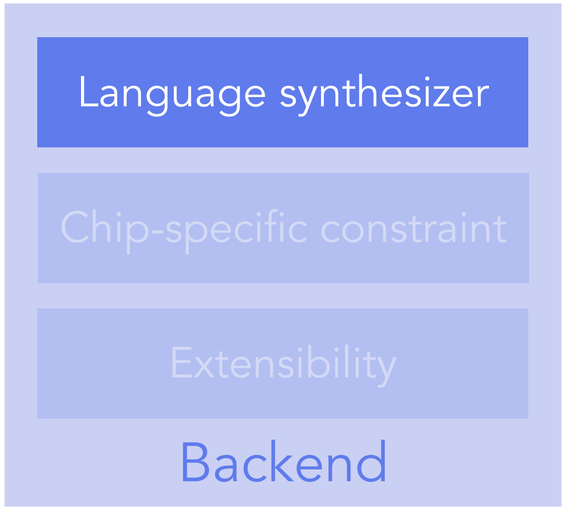


Lyra: A high-level data plane language & compiler

Alibaba Cloud
Worldwide Cloud Services Partner



→ **Portability |** Compile Lyra into structured low level languages

→ **Composition |** Checks whether the program can fit into the switch

→ **Extensibility |** Correctly deploy the program in the scope

Lyra: A high-level data plane language & compiler

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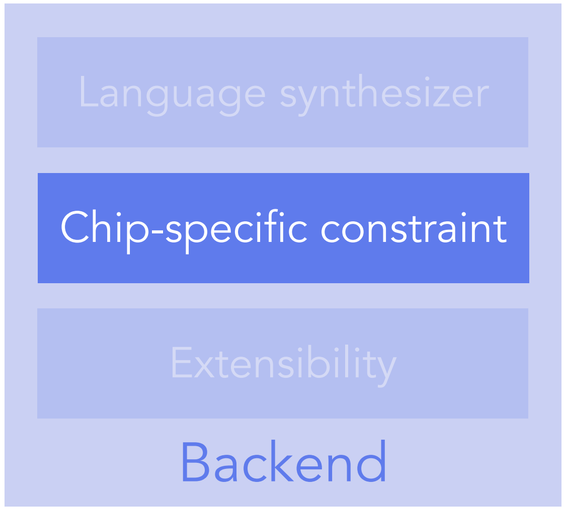

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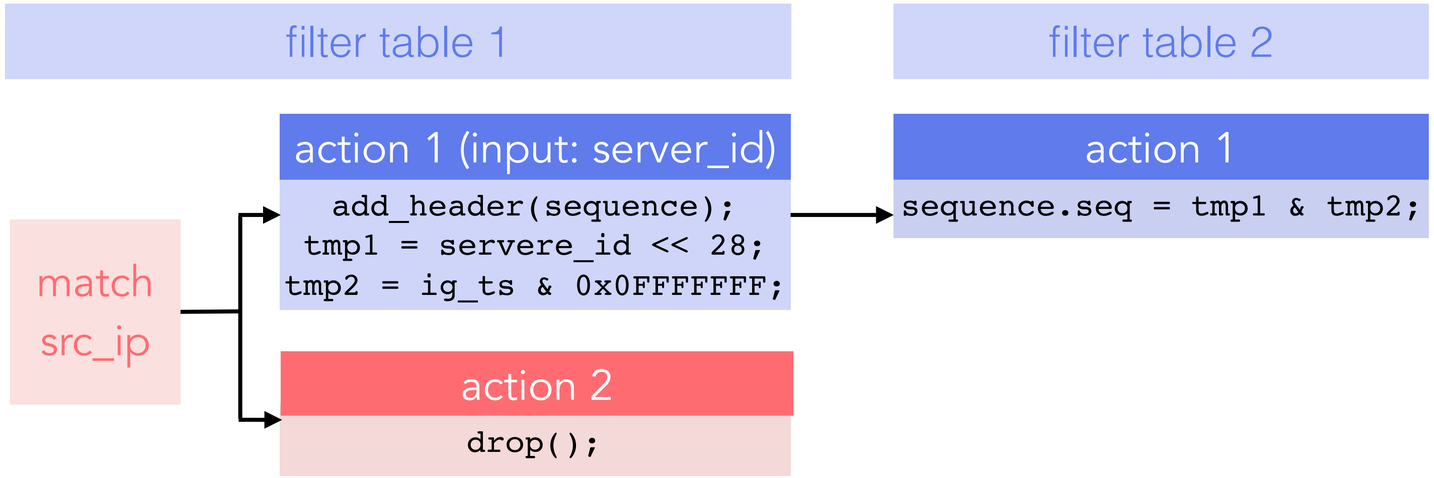
Target-specific resource encoding: RMT



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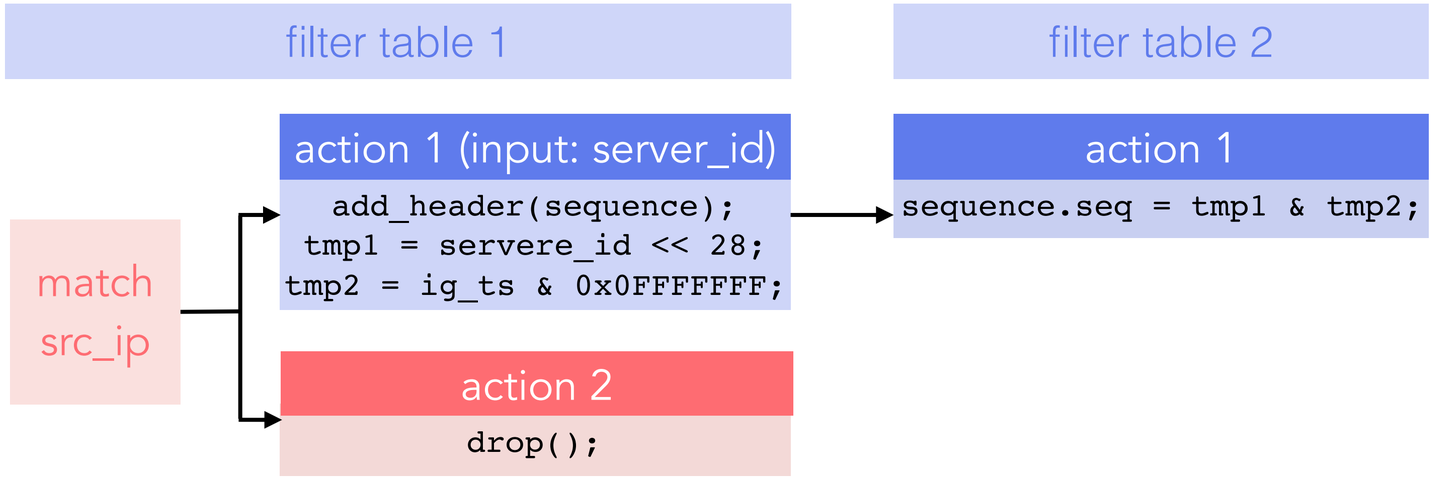
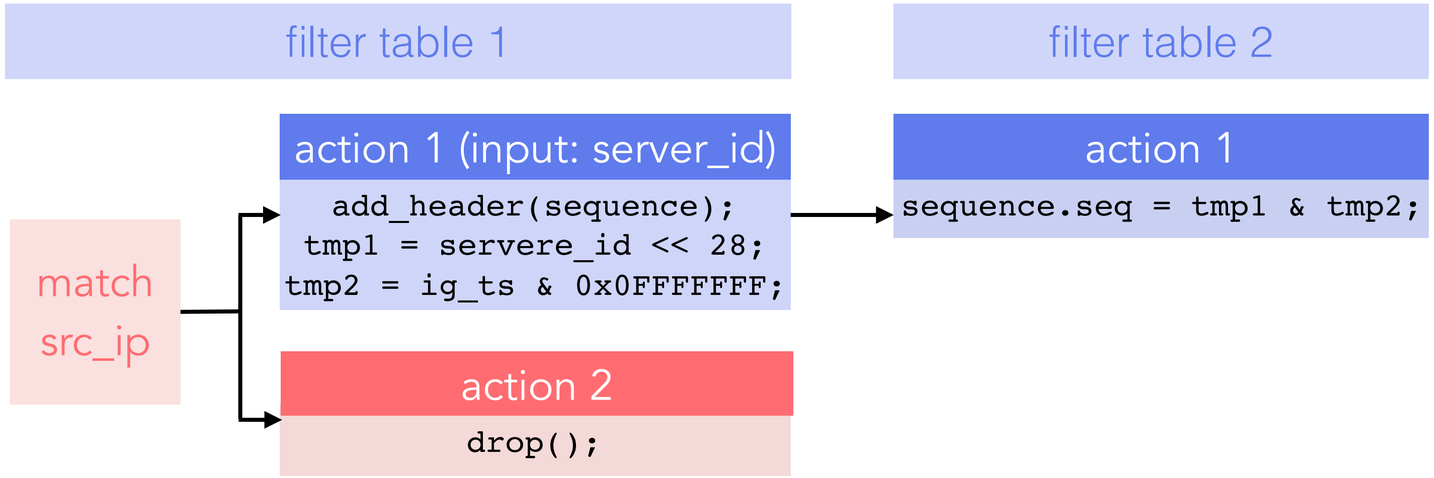


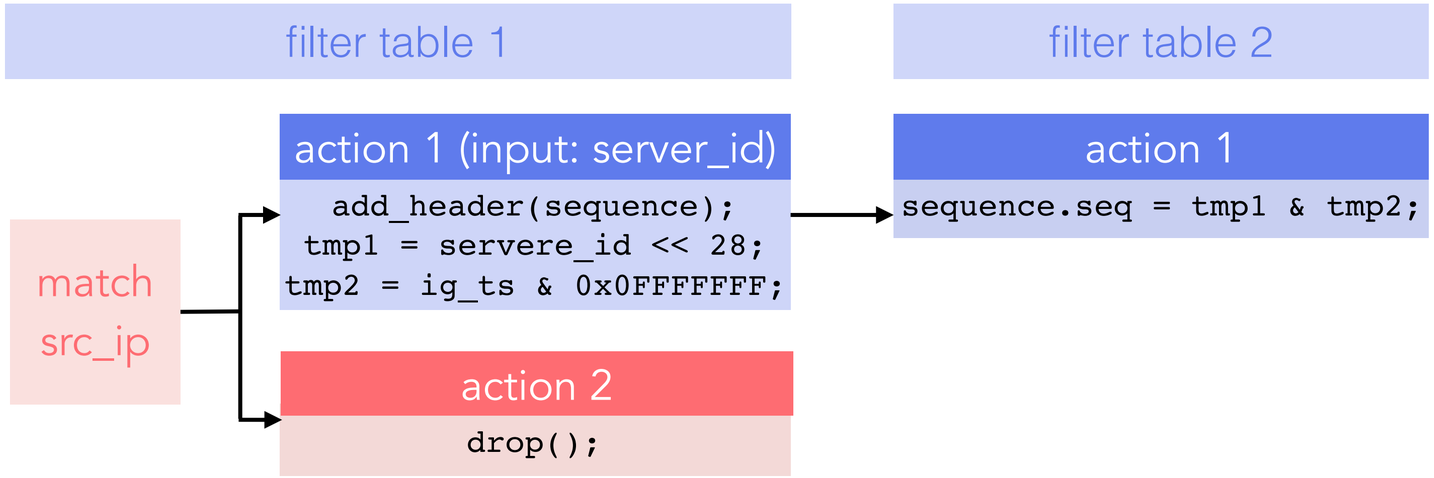
S_{filter_1} S_{filter_2}

Target-specific resource encoding: RMT



$$S_{filter_1} < S_{filter_2}$$

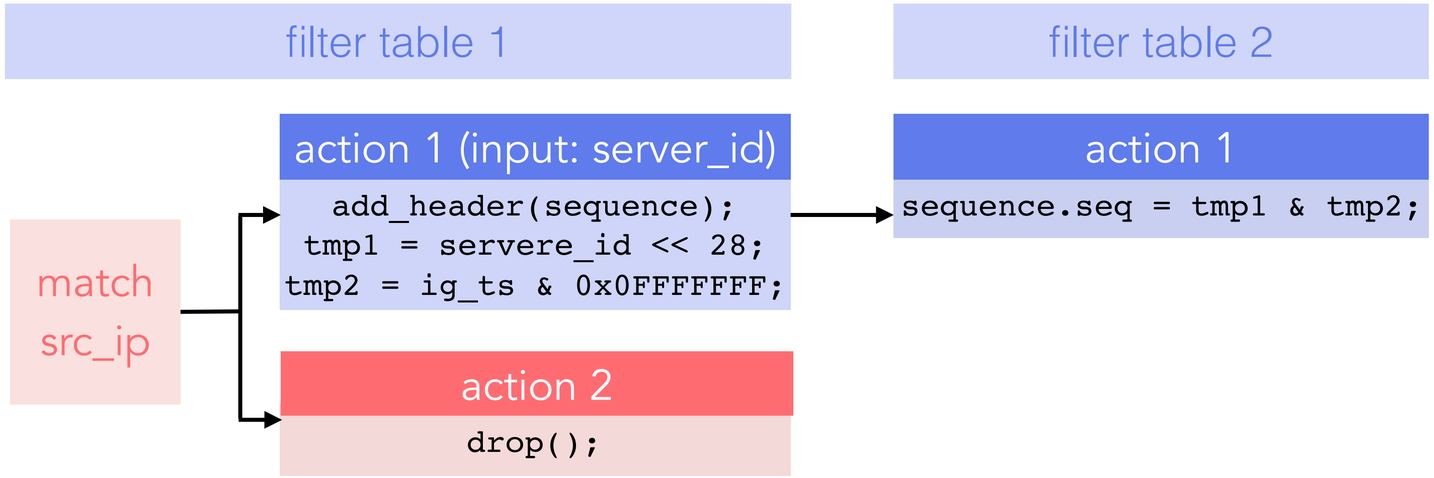
Target-specific resource encoding: RMT



$$S_{filter_1} < S_{filter_2}$$

$$0 \leq S_{filter_1} \leq 31$$

Target-specific resource encoding: RMT



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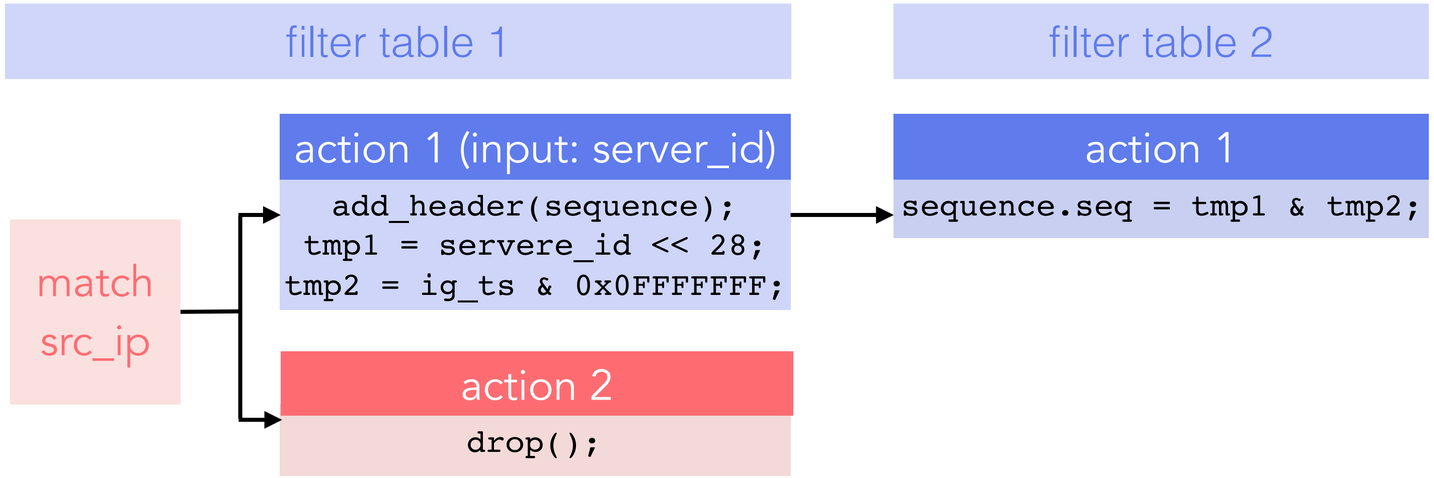

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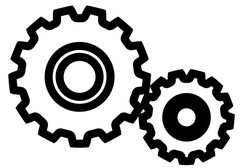
SMT solver



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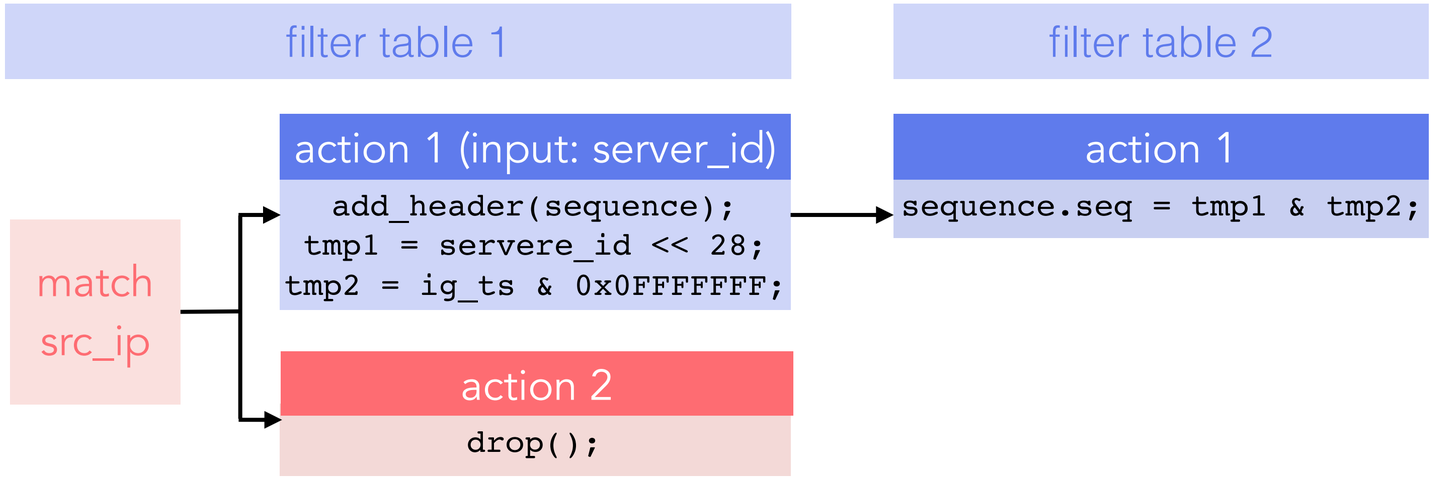

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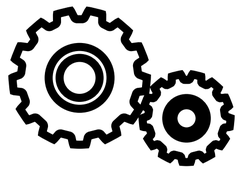
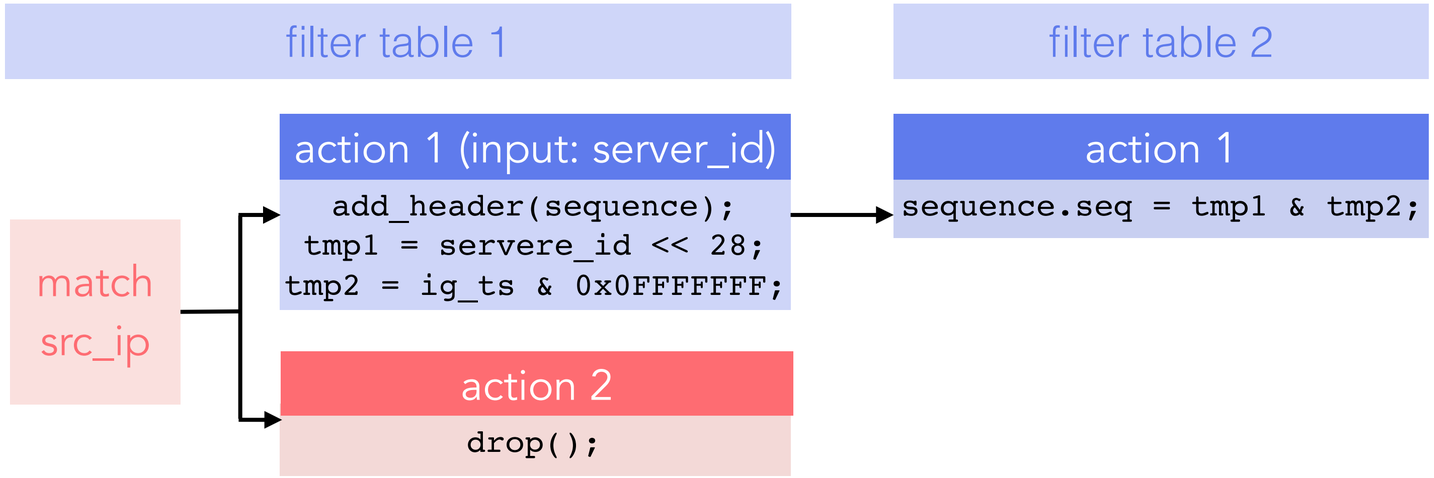


$$S_{filter_1} = 0$$

$$S_{filter_2} = 1$$

Target-specific resource encoding: RMT



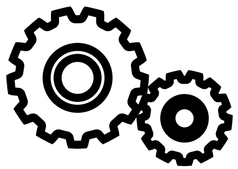
- SRAM memory
- TCAM memory
- Packet Header Vector
- Table num per stage

$$S_{filter_1} < S_{filter_2}$$

$$0 \leq S_{filter_1} \leq 31$$

$$0 \leq S_{filter_2} \leq 31$$

SMT solver



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Lyra: A high-level data plane language & compiler

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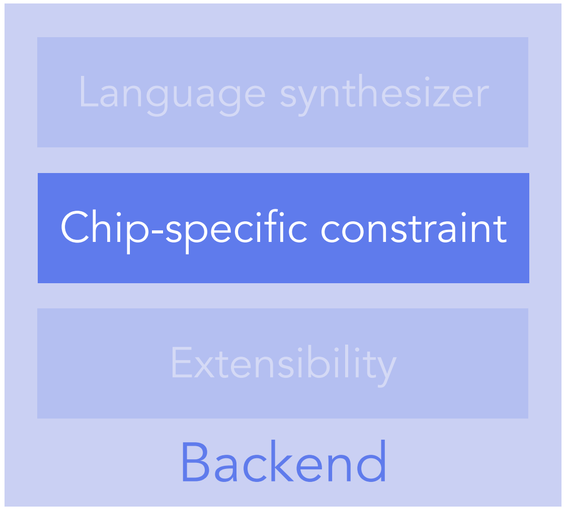

→ **Portability |** Compile Lyra into structured low level languages

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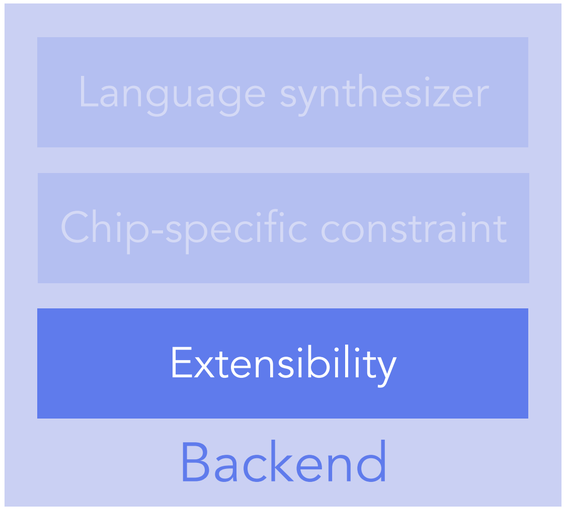

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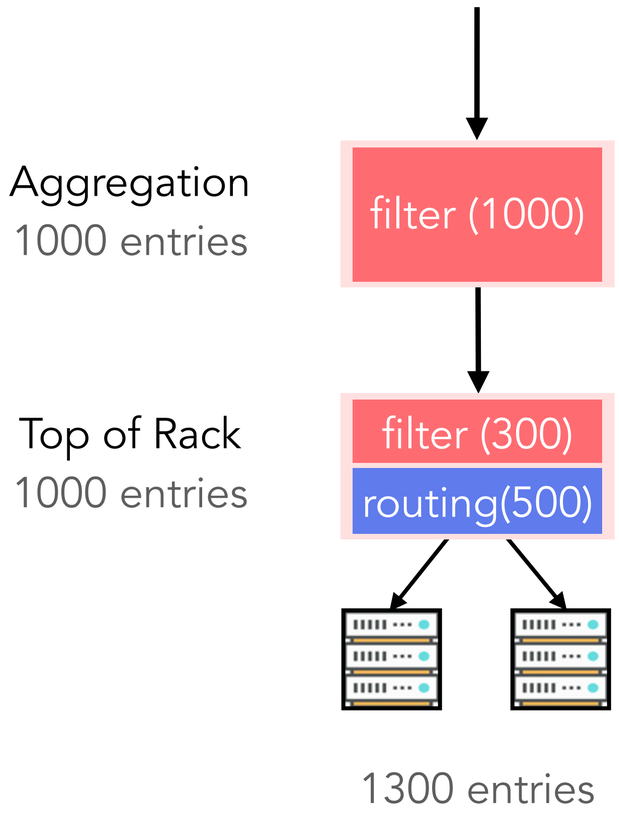
Pass information between switches

Pass information between switches

Pack downstream switches' required data into packet header

Pass information between switches

Pack downstream switches' required data into packet header



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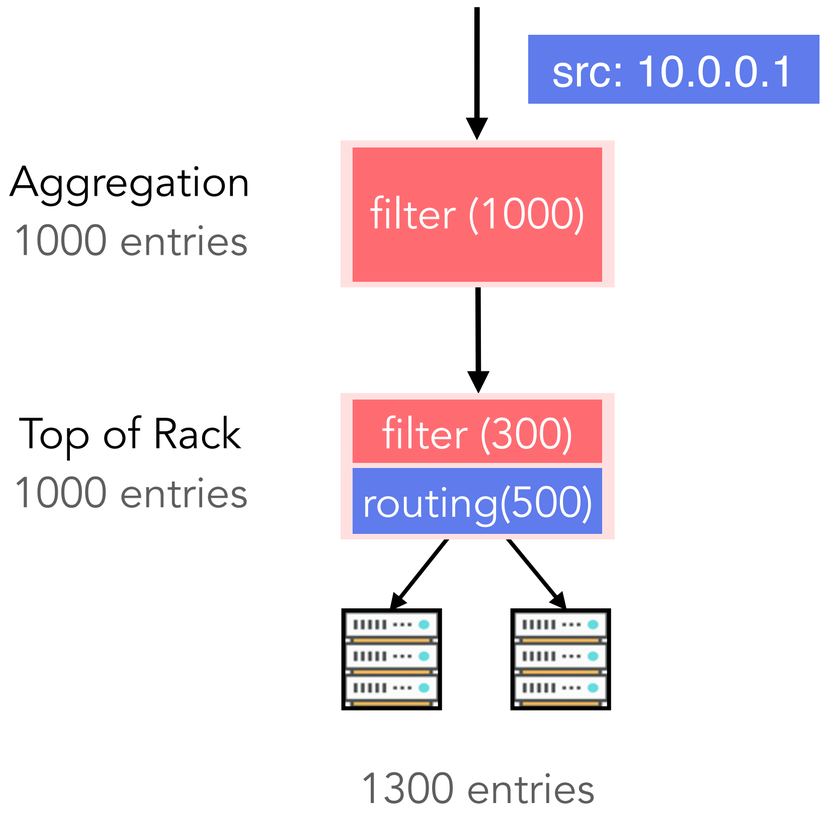

Pass information between switches

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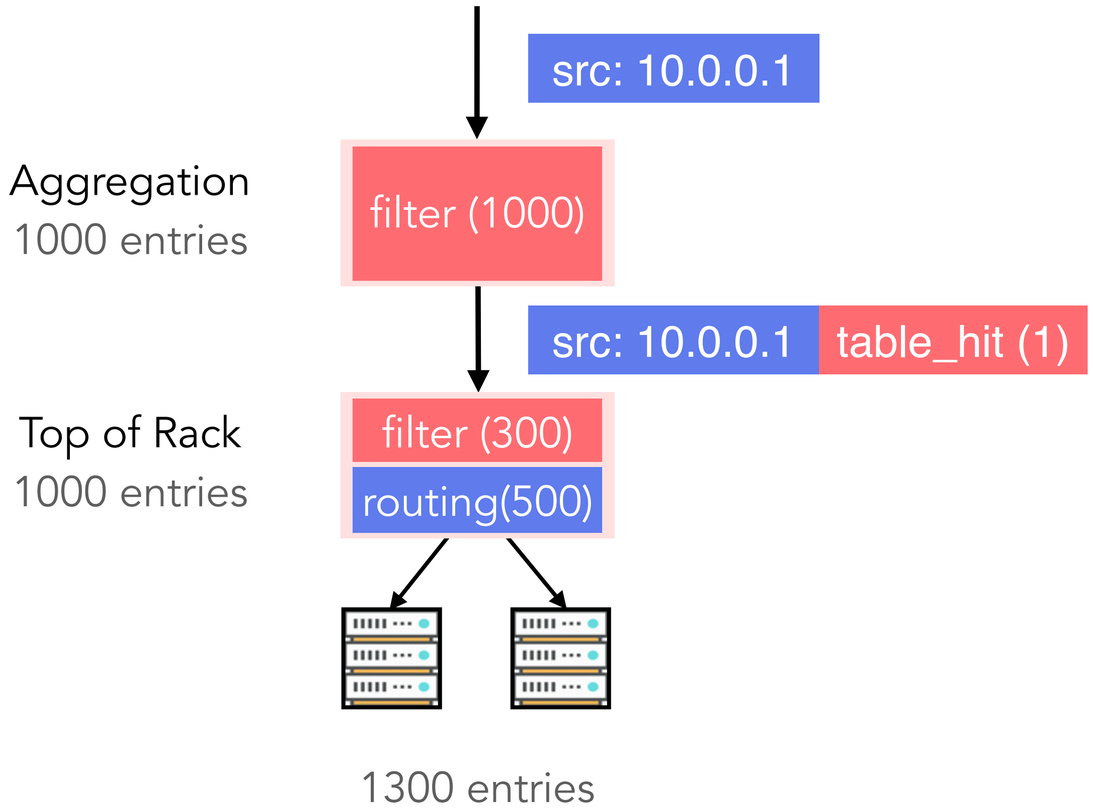
Pack downstream switches' required data into packet header



Pass information between switches

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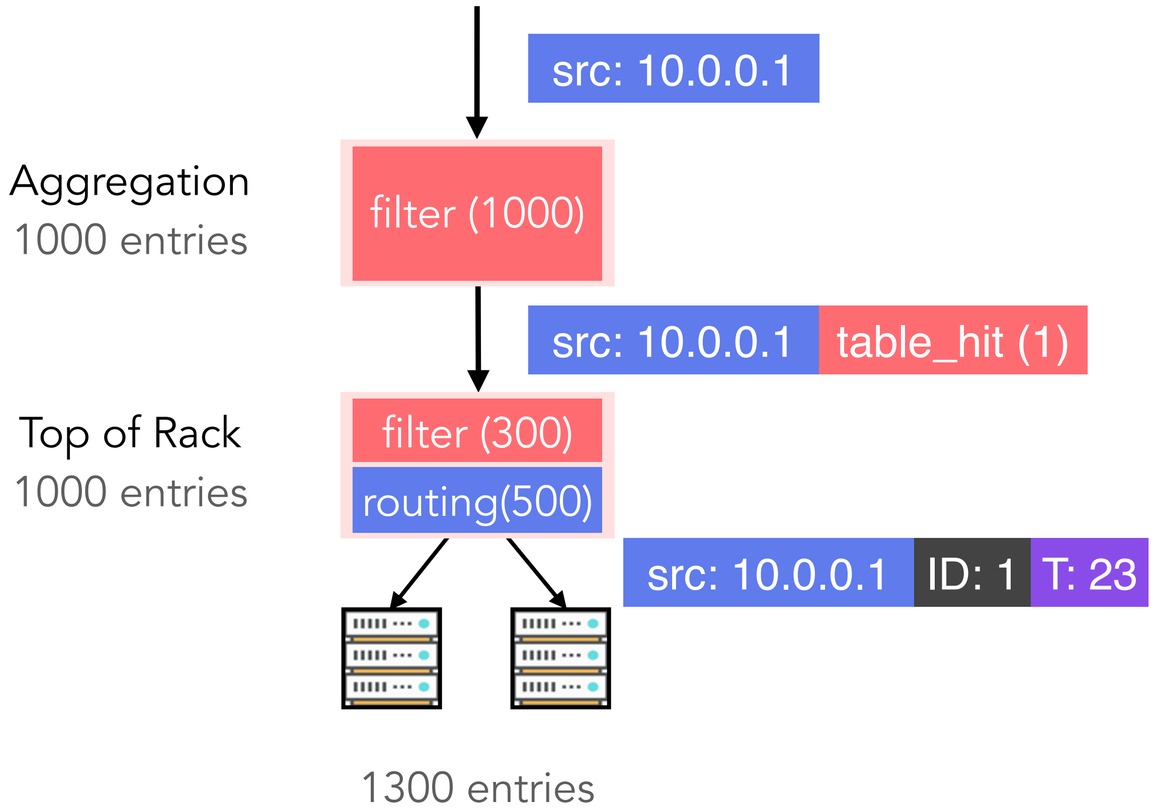
Pack downstream switches' required data into packet header



Pass information between switches

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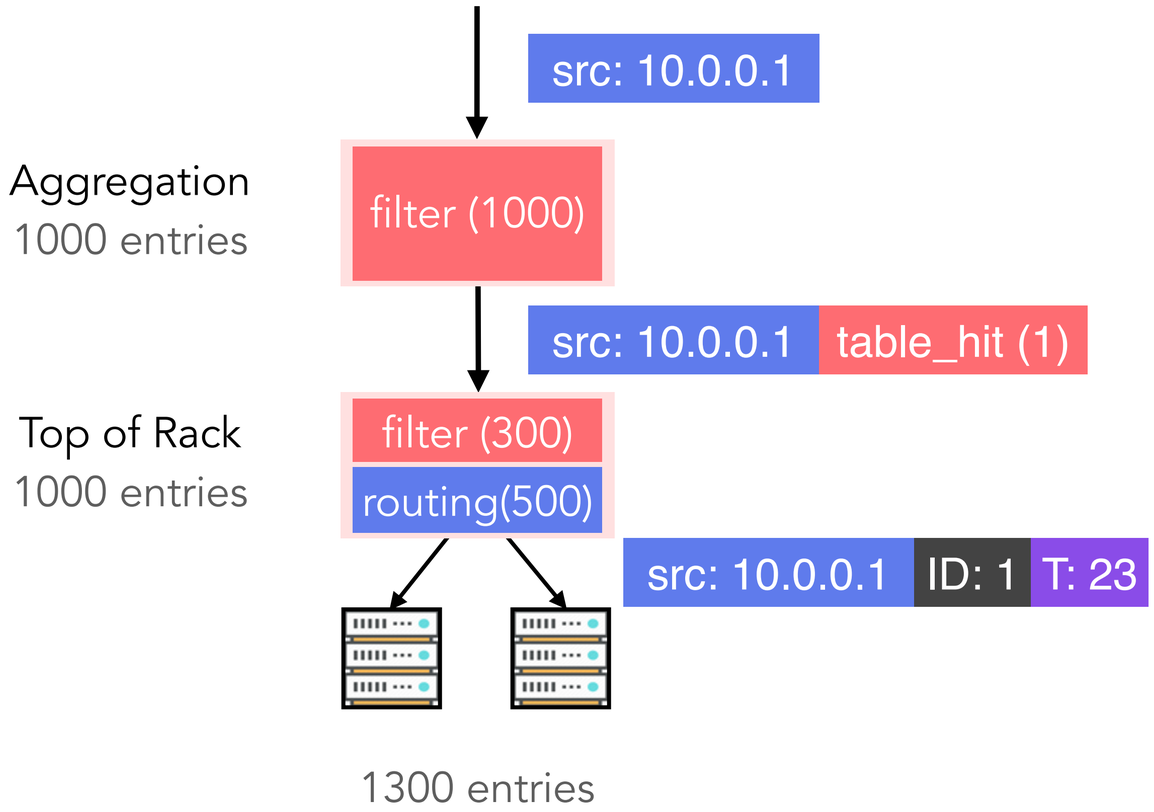
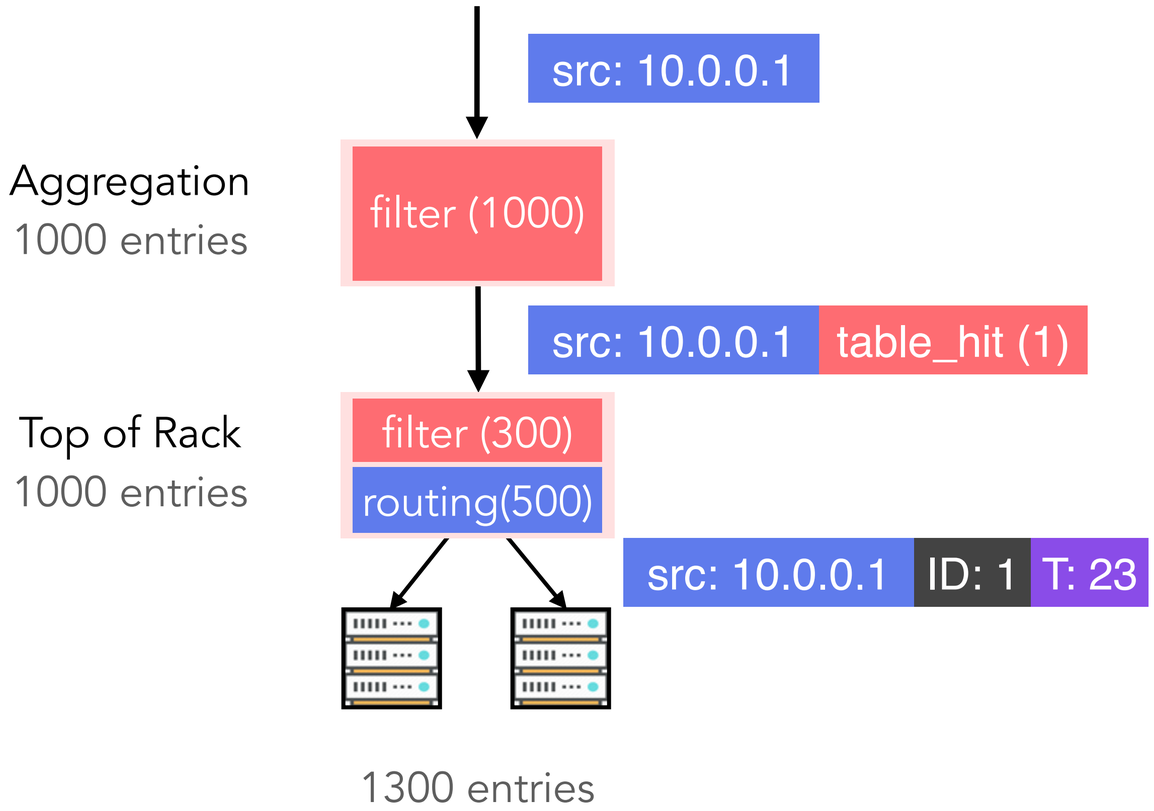


No code is duplicated

Pass information between switches

Pack downstream switches' required data into packet header

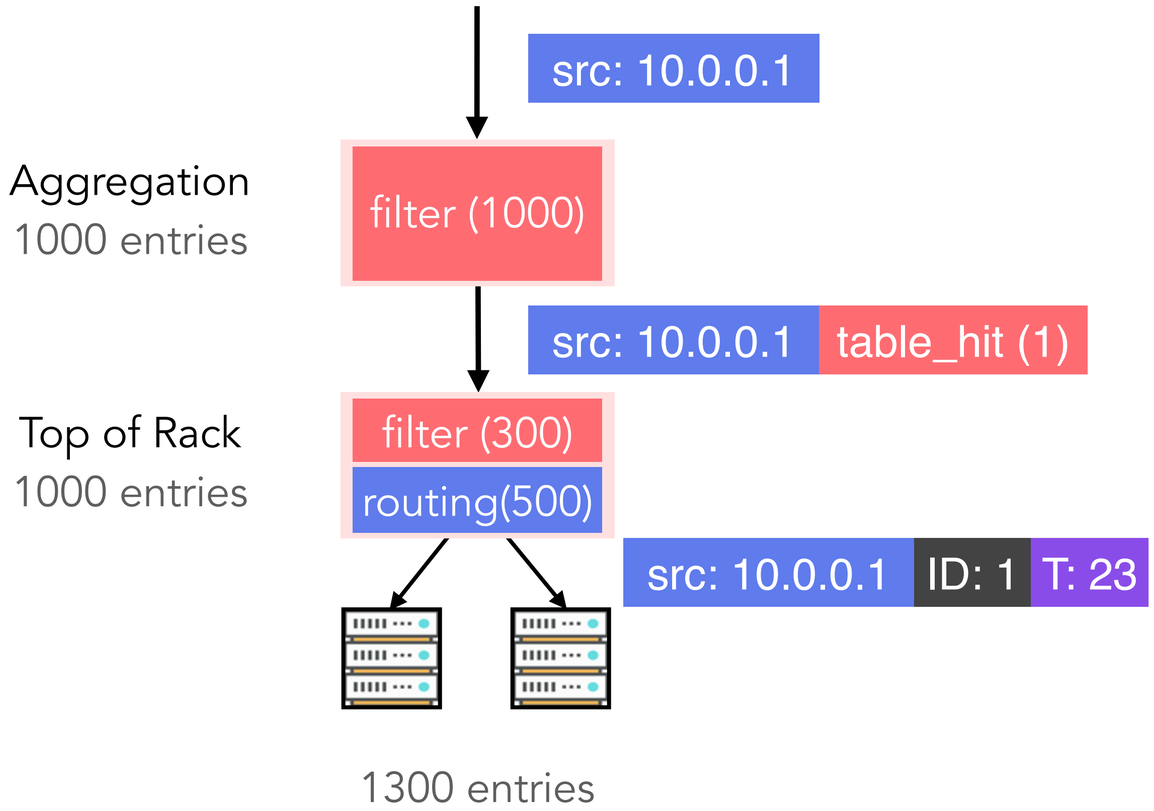


No code is duplicated

No code is missing

Pass information between switches

Pack downstream switches' required data into packet header



No code is duplicated

No code is missing

No reordering

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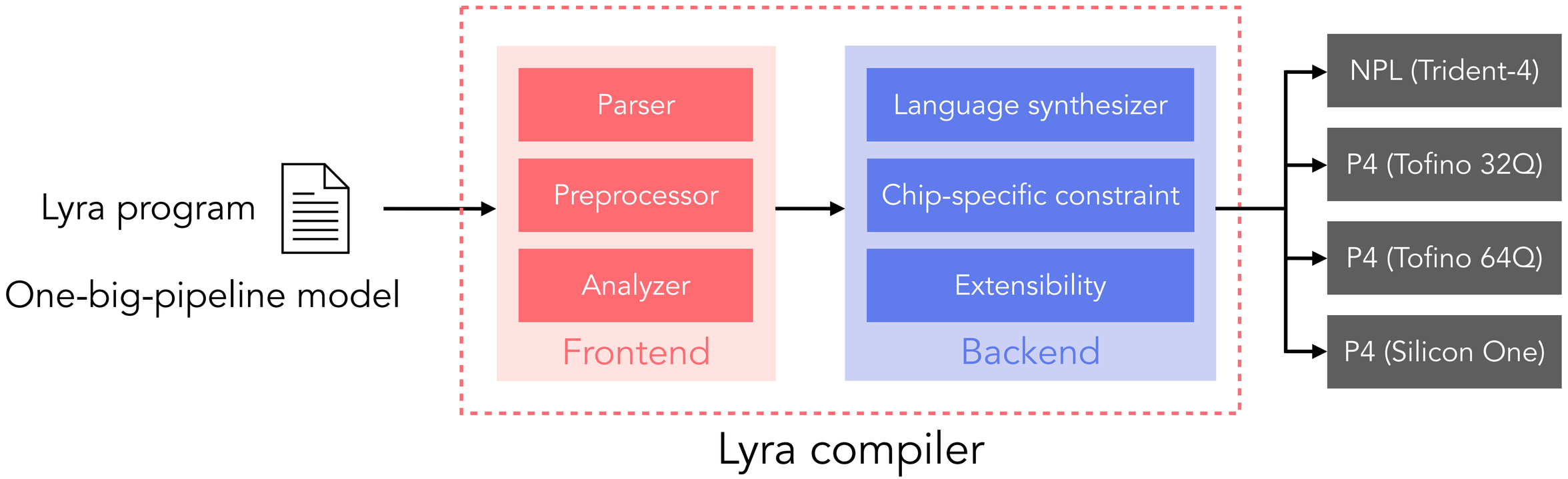

Evaluation

Demo for portability, extensibility and composition

Lyra can reduce resource usage

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Program	P4$_{14}$				Lyra								
						Synthesized P4$_{14}$				Synthesized NPL			
	LoC / Logic LoC	Tables	Actions	Registers	Lyra LoC / Logic LoC	Lyra Compile Time	Tables	Actions	Registers	Lyra Compile Time	Tables	Registers	Longest Code Path
Ingress INT	308/99	9	8	0	207/62	0.987s	8	7	0	0.78s	4	0	9
Transit INT	275/66	6	6	0	193/46	0.914s	5	5	0	0.72s	2	0	4
Egress INT	282/73	7	7	0	197/47	0.897s	6	6	0	0.73s	2	0	4
Speedlight	453/351	21	23	6	194/97	1.352s	16	20	6	0.95s	9	6	18
NetCache	1137/937	96	96	40	372/153	1.909s	12	14	40	1.17s	3	40	20
NetChain	319/211	16	16	2	177/73	1.530s	13	16	2	0.85s	6	2	18
NetPaxos	241/140	6	11	5	150/69	1.158s	6	11	5	0.84s	3	5	4
flowlet_switching	195/130	8	7	2	113/43	0.91s	8	7	2	0.70s	4	2	12
simple_router	101/66	4	4	0	72/31	0.852s	4	4	0	0.67s	3	0	10
switch	4924/3876	131	363	0	4151/2563	33.6s	131	363	0	19.4s	125	0	53

Lyra can reduce resource usage

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Program	$P4_{14}$				Lyra								
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Egress INT	282/73	7	7	0	197/47	0.897s	6	6	0	0.73s	2	0	4
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Lyra can reduce resource usage

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Lyra can reduce resource usage

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Speedlight	453/351	21	23	6	194/97	1.352s	16	20	6	0.95s	9	6	18
NetCache	1137/937	96	96	40	372/153	1.909s	12	14	40	1.17s	3	40	20
NetChain	319/211	16	16	2	177/73	1.530s	13	16	2	0.85s	6	2	18
NetPaxos	241/140	6	11	5	150/69	1.158s	6	11	5	0.84s	3	5	4
flowlet_switching	195/130	8	7	2	113/43	0.91s	8	7	2	0.70s	4	2	12
simple_router	101/66	4	4	0	72/31	0.852s	4	4	0	0.67s	3	0	10
switch	4924/3876	131	363	0	4151/2563	33.6s	131	363	0	19.4s	125	0	53

Lyra can reduce resource usage

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Program	P4$_{14}$				Lyra								
						Synthesized P4$_{14}$				Synthesized NPL			
	LoC / Logic LoC	Tables	Actions	Registers	Lyra LoC / Logic LoC	Lyra Compile Time	Tables	Actions	Registers	Lyra Compile Time	Tables	Registers	Longest Code Path
Ingress INT	308/99	9	8	0	207/62	0.987s	8	7	0	0.78s	4	0	9
Transit INT	275/66	6	6	0	193/46	0.914s	5	5	0	0.72s	2	0	4
Egress INT	282/73	7	7	0	197/47	0.897s	6	6	0	0.73s	2	0	4
Speedlight	453/351	21	23	6	194/97	1.352s	16	20	6	0.95s	9	6	18
NetCache	1137/937	96	96	40	372/153	1.909s	12	14	40	1.17s	3	40	20
NetChain	319/211	16	16	2	177/73	1.530s	13	16	2	0.85s	6	2	18
NetPaxos	241/140	6	11	5	150/69	1.158s	6	11	5	0.84s	3	5	4
flowlet_switching	195/130	8	7	2	113/43	0.91s	8	7	2	0.70s	4	2	12
simple_router	101/66	4	4	0	72/31	0.852s	4	4	0	0.67s	3	0	10
switch	4924/3876	131	363	0	4151/2563	33.6s	131	363	0	19.4s	125	0	53

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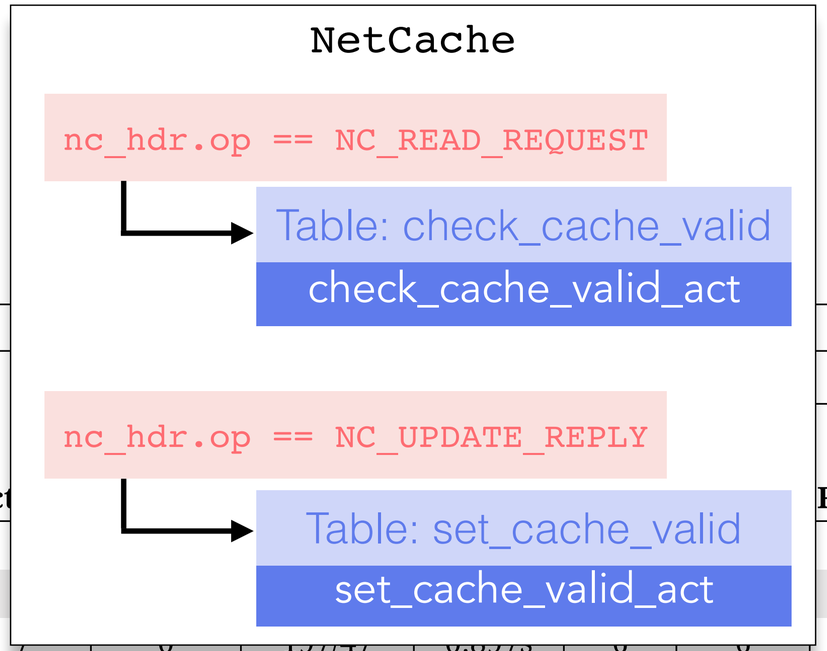
Lyra can reduce resource usage



Program	$P4_{14}$								Lyra				
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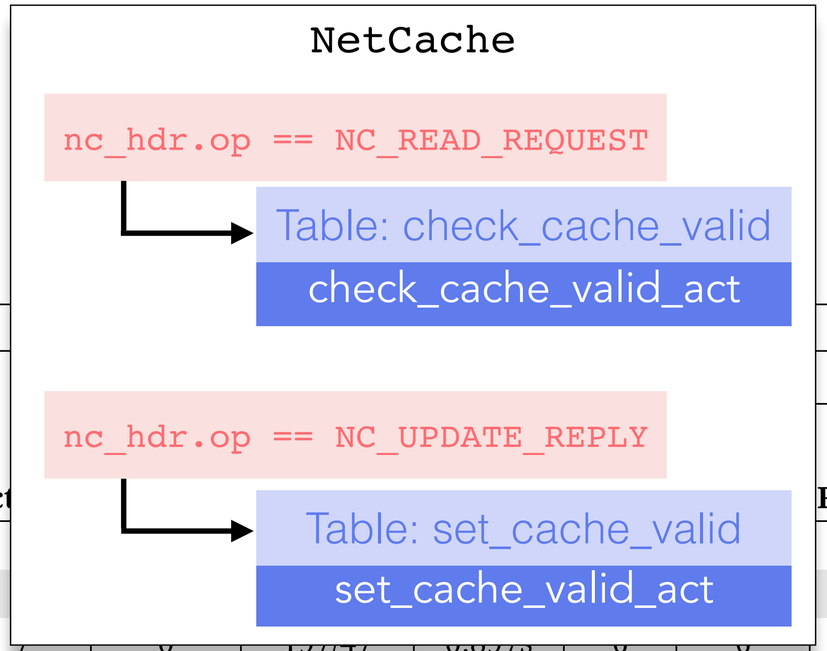

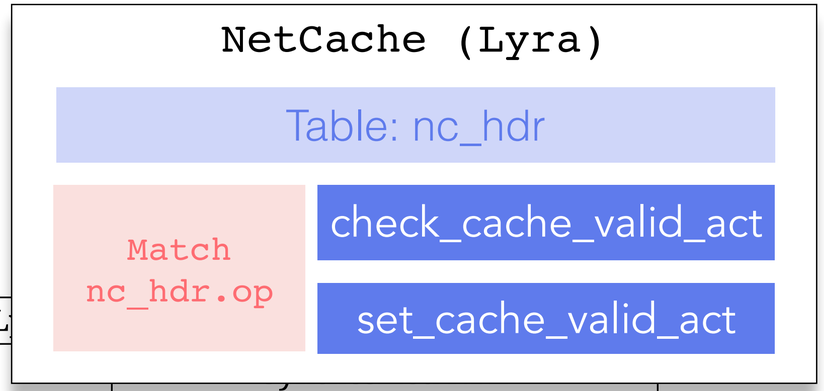

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Conclusion

- Lyra is the first high-level data plane language and compiler that achieves portability, extensibility and composition.
- Lyra offers a one-big-pipeline programming model and can generate runnable chip-specific code across multiple switches.
- The programs generated by Lyra use fewer hardware resources than human-written programs.

Thanks !